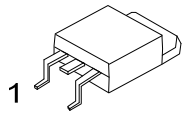
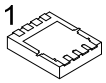
48A, 120V N-CHANNEL POWER MOSFET



TO-252



PDFN5×6

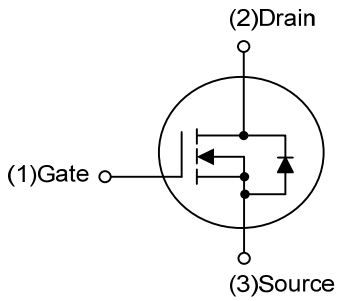
■ DESCRIPTION

The UTC **UT48N12H** is a is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

■ FEATURES

* $R_{DS(ON)} \leq 20\ m\Omega$ @ V_{GS}=10V, I_D=24A
* Improved dv/dt capability
* High Switching Speed
* Fast switching

■ SYMBOL



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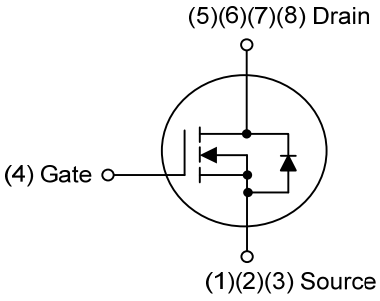


PDFN5×6

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT48N12HL-TN3-R	UT48N12HG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT48N12HL-P5060-R	UT48N12HG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

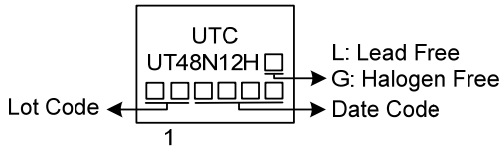
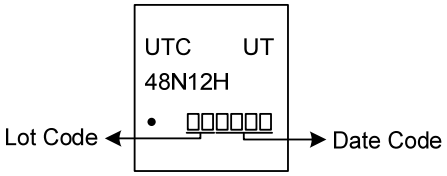
UT48N12HG-TN3-R

(1)Packing Type — (1) R: Tape Reel

(2)Package Type — (2) TN3: TO-252, P5060: PDFN5×6

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

TO-252	PDFN5×6
	

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	120	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	48	A
	Pulsed (Note 2)	I_{DM}	96	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	67	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	7	V/ns
Power Dissipation	TO-252	P_D	18	W
	PDFN5×6		48	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 0.1mH, I_{AS} = 36.7A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C.
4. I_{SD} ≤ 30A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	°C/W
	PDFN5×6		83	°C/W
Junction to Case	TO-252	θ_{JC}	2.6	°C/W
	PDFN5×6		8.9	°C/W

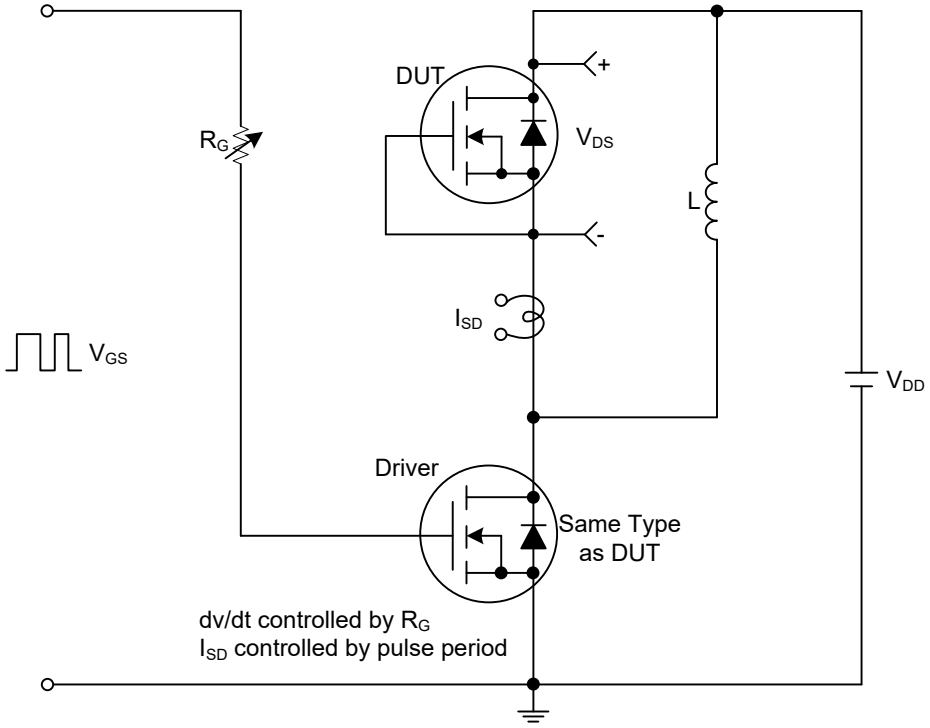
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

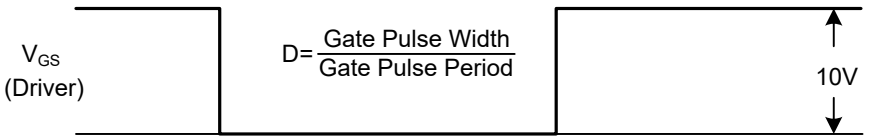
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

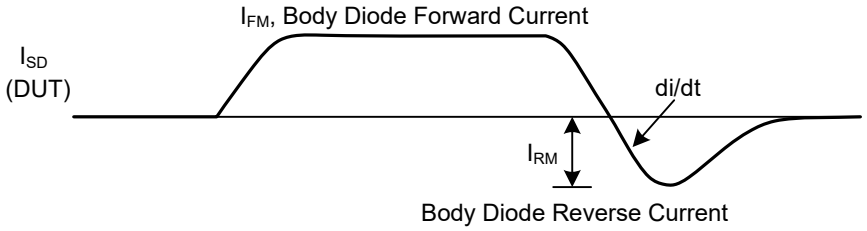
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250μA	120			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=120V, V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=24A			20	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		3869		pF
Output Capacitance		C_{OSS}			287		pF
Reverse Transfer Capacitance		C_{RSS}			247		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{DS}=96V, V_{GS}=10V, I_D=48A (Note 2)		122		nC
Gate to Source Charge		Q_{GS}			35		nC
Gate to Drain Charge		Q_{GD}			40		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=60V, V_{GS}=10V, I_D=48A, R_G=3Ω, (Note 2)		20		ns
Rise Time		t_R			21		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			79		ns
Fall-Time		t_F			33		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I_S				48	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}				96	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=48A,V_{GS}=0V			1.4	V
Body Diode Reverse Recovery Time		t_{rr}	I_F=30A,V_{GS}=0V, di/dt=100A/μs		83		ns
Body Diode Reverse Recovery Charge		Q_{rr}			162		nC

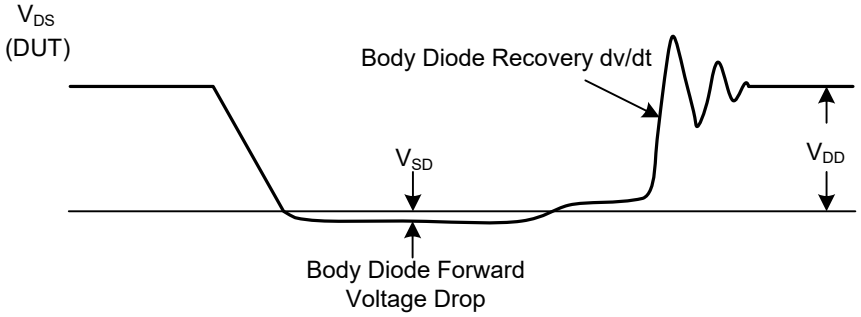
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



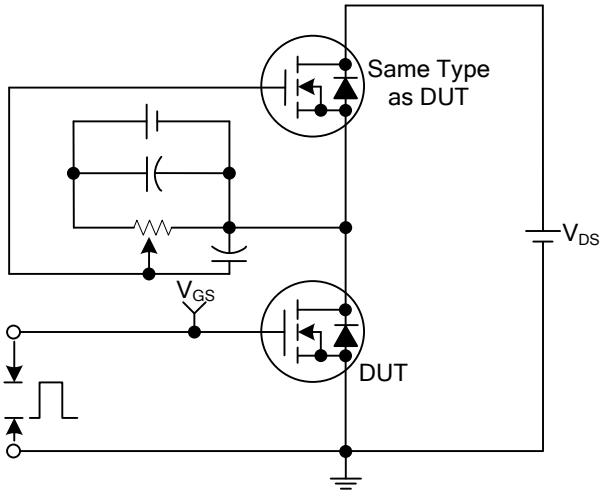




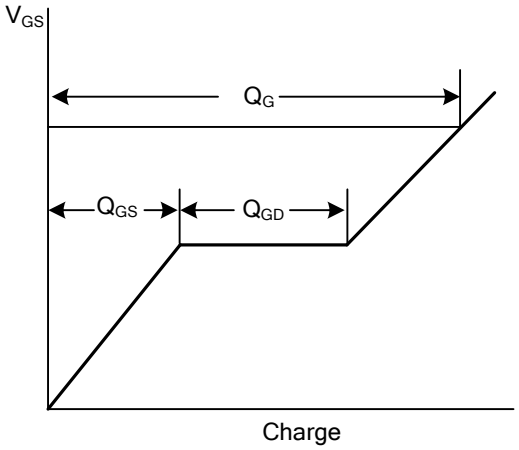


Peak Diode Recovery dv/dt Test Circuit and Waveforms

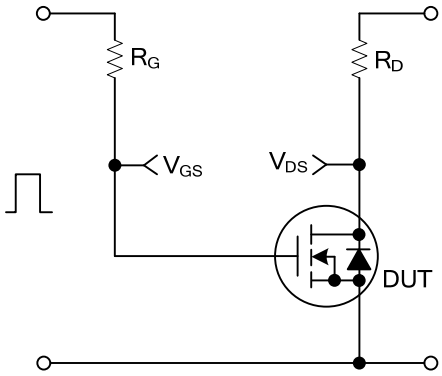
■ TEST CIRCUITS AND WAVEFORMS



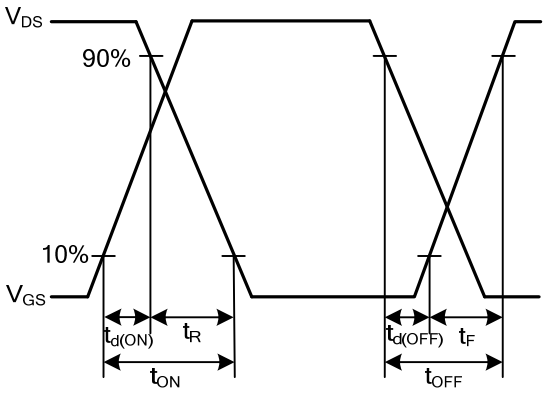
Gate Charge Test Circuit



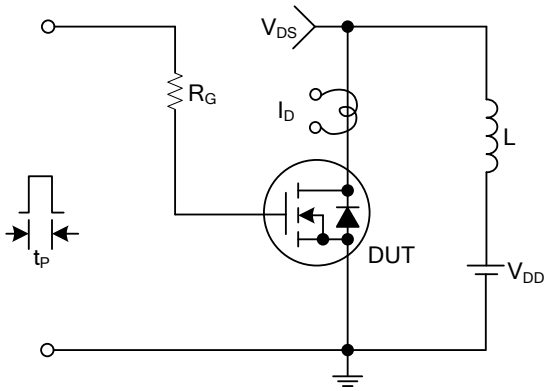
Gate Charge Waveforms



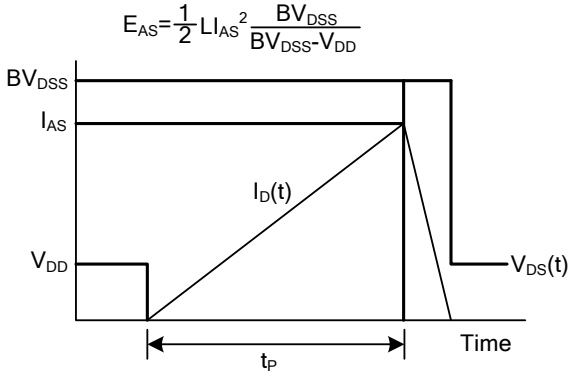
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms