



UT48N12H

Preliminary

Power MOSFET

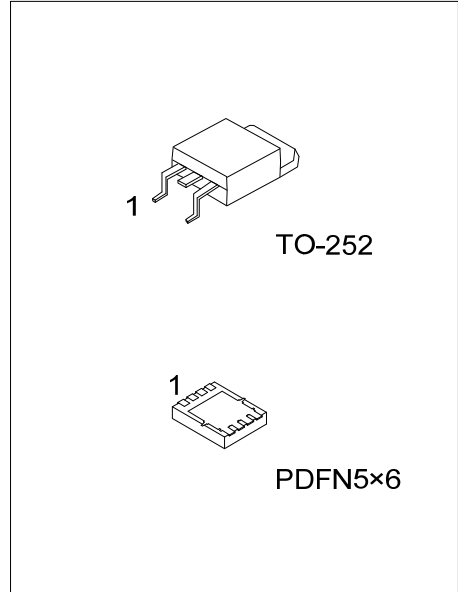
**48A, 120V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

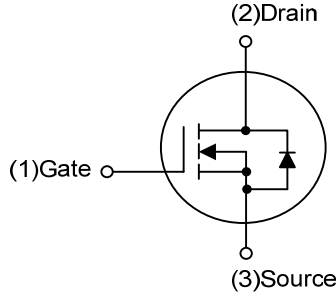
The UTC **UT48N12H** is a N-Channel enhancement mode power field effect transistors using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

■ FEATURES

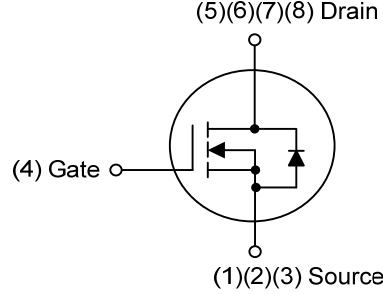
- * $R_{DS(ON)} \leq 20 \text{ m}\Omega$ @ $V_{GS}=10V, I_D=24A$
- * Improved dv/dt capability
- * High Switching Speed
- * Fast switching



■ SYMBOL



TO-252



PDFN5x6

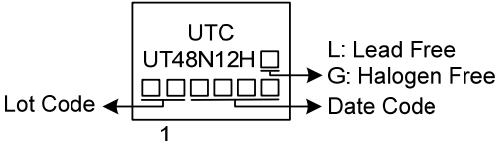
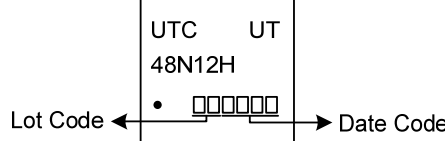
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
UT48N12HL-TN3-R	UT48N12HG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT48N12HL-P5060-R	UT48N12HG-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT48N12HG-TN3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252, P5060: PDFN5x6</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

TO-252	PDFN5x6
 <p>The diagram shows a rectangular marking area for a TO-252 package. It contains the text 'UTC' and 'UT48N12H' followed by a small square. Below this is a row of five squares, with the first one labeled 'Lot Code' and the last one labeled 'Date Code'. To the right of the row are the labels 'L: Lead Free' and 'G: Halogen Free'. A '1' is centered below the row of squares.</p>	 <p>The diagram shows a rectangular marking area for a PDFN5x6 package. It contains the text 'UTC UT' and '48N12H' followed by a small square. Below this is a row of five squares, with the first one labeled 'Lot Code' and the last one labeled 'Date Code'. A dot is positioned to the left of the row of squares.</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	120	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	48	A
	Pulsed (Note 2)	I_{DM}	96	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	67	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	7	V/ns
Power Dissipation	TO-252	P_D	18	W
	PDFN5x6		48	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 36.7\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^\circ\text{C}/\text{W}$
	PDFN5x6		83	$^\circ\text{C}/\text{W}$
Junction to Case	TO-252	θ_{JC}	2.6	$^\circ\text{C}/\text{W}$
	PDFN5x6		8.9	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

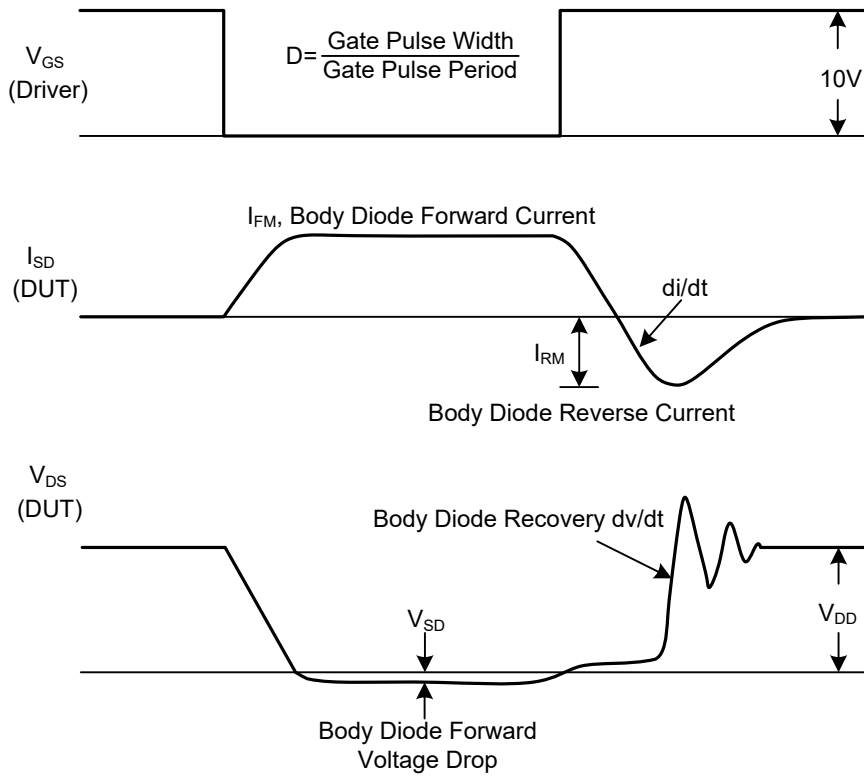
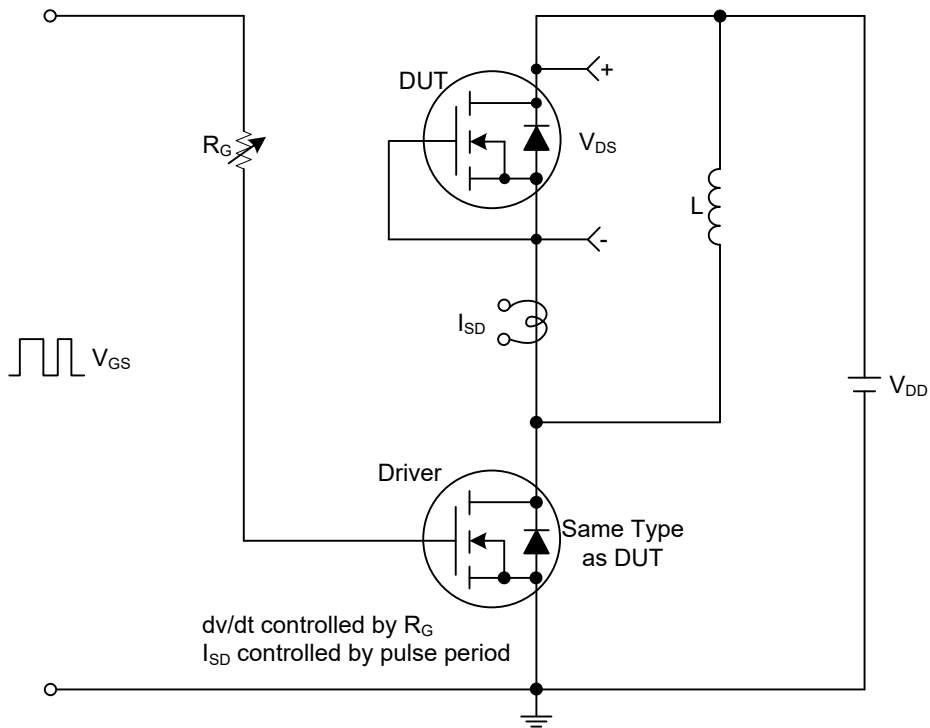
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	120			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =120V, V _{GS} =0V			1	μA
Gate- Source Leakage Current	Forward	I _{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =24A			20	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		3869		pF
Output Capacitance	C _{OSS}			287		pF
Reverse Transfer Capacitance	C _{RSS}			247		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =96V, V _{GS} =10V, I _D =48A (Note 2)		122		nC
Gate to Source Charge	Q _{GS}			35		nC
Gate to Drain Charge	Q _{GD}			40		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =60V, V _{GS} =10V, I _D =48A, R _G =3Ω, (Note 2)		20		ns
Rise Time	t _R			21		ns
Turn-OFF Delay Time	t _{D(OFF)}			79		ns
Fall-Time	t _F			33		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				48	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				96	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =48A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time	t _{rr}	I _F =30A, V _{GS} =0V, di/dt=100A/μs		83		ns
Body Diode Reverse Recovery Charge	Q _{rr}			162		nC

Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

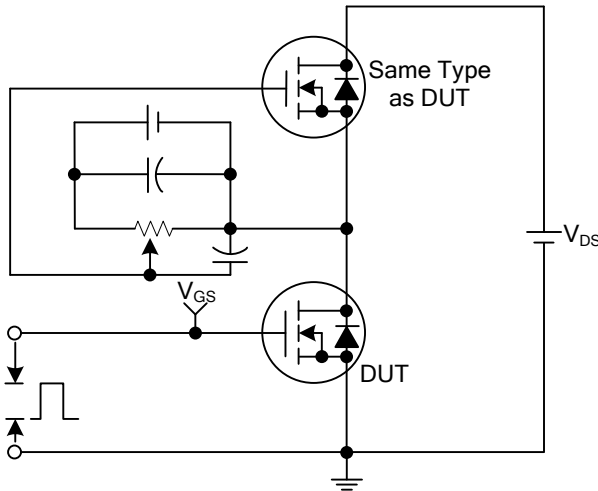
2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

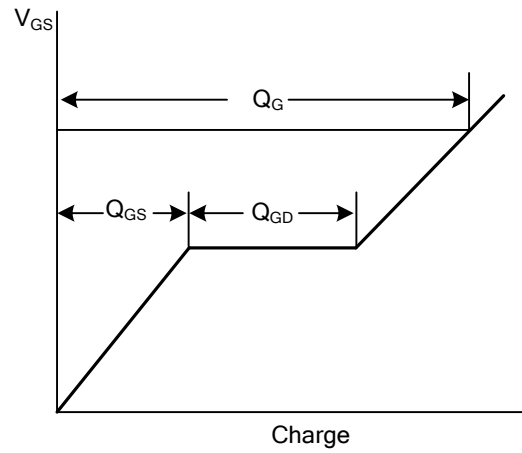


Peak Diode Recovery dv/dt Test Circuit and Waveforms

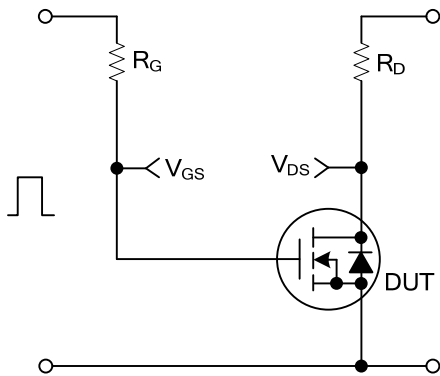
■ TEST CIRCUITS AND WAVEFORMS



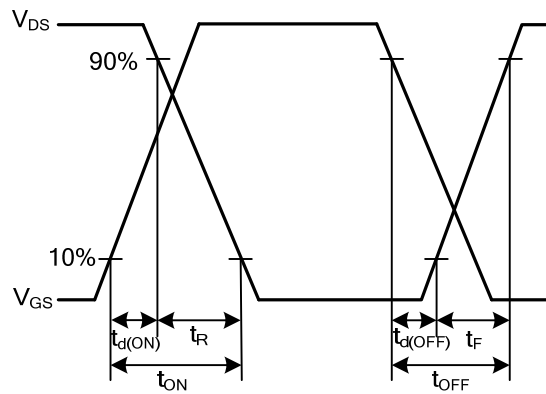
Gate Charge Test Circuit



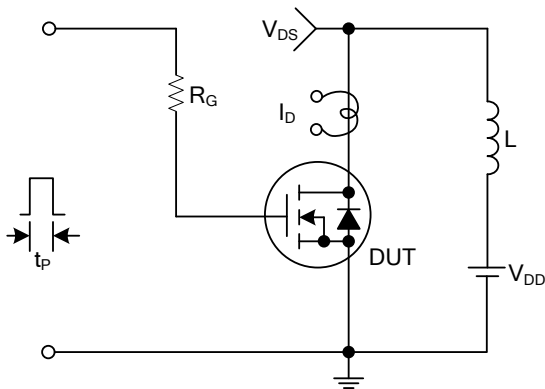
Gate Charge Waveforms



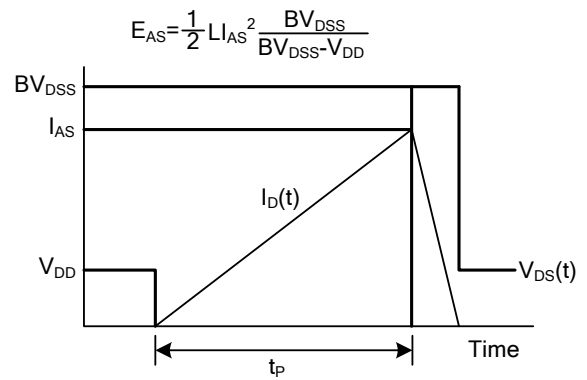
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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