

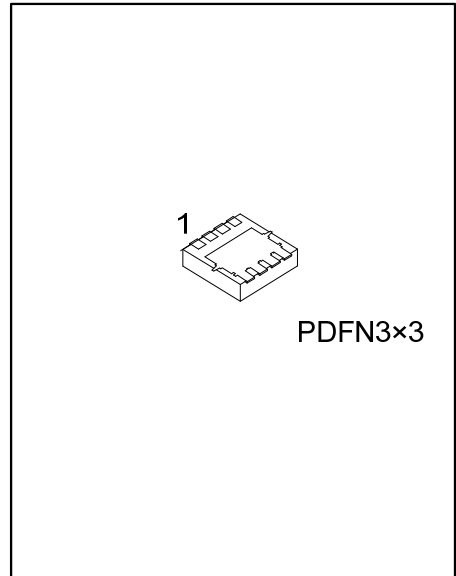


USG10R135M

Preliminary

Power MOSFET

**N-CHANNEL SGT
ENHANCEMENT POWER
MOSFET**



■ DESCRIPTION

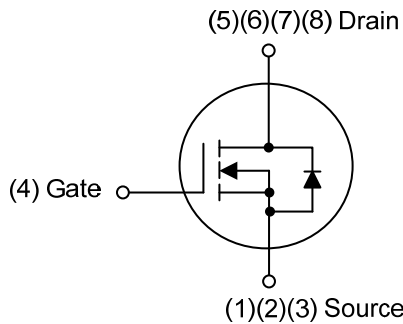
The UTC **USG10R135M** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with high switching speed and low gate charge, etc.

The UTC **USG10R135M** applies to primary side switch, synchronous rectifier, Motor Drives, etc.

■ FEATURES

- * $R_{DS(ON)} \leq 13.5\text{ m}\Omega$ @ $V_{GS}=10V, I_D=20A$
- $R_{DS(ON)} \leq 22\text{ m}\Omega$ @ $V_{GS}=4.5V, I_D=20A$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

■ SYMBOL



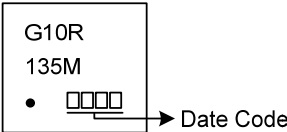
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
USG10R135ML-P3030-R	USG10R135MG-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

<p>USG10R135MG-P3030-R</p>	<p>(1) R: Tape Reel</p> <p>(2) P3030: PDFN3x3</p> <p>(3) G: Halogen Free and Lead Free, K: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	45	A
	Pulsed (Note 2)	I_{DM}	90	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	5.4	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	0.9	V/ns
Power Dissipation		P_D	25	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

3. $L = 0.1\text{mH}$, $I_{AS} = 10.4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	130	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	5	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

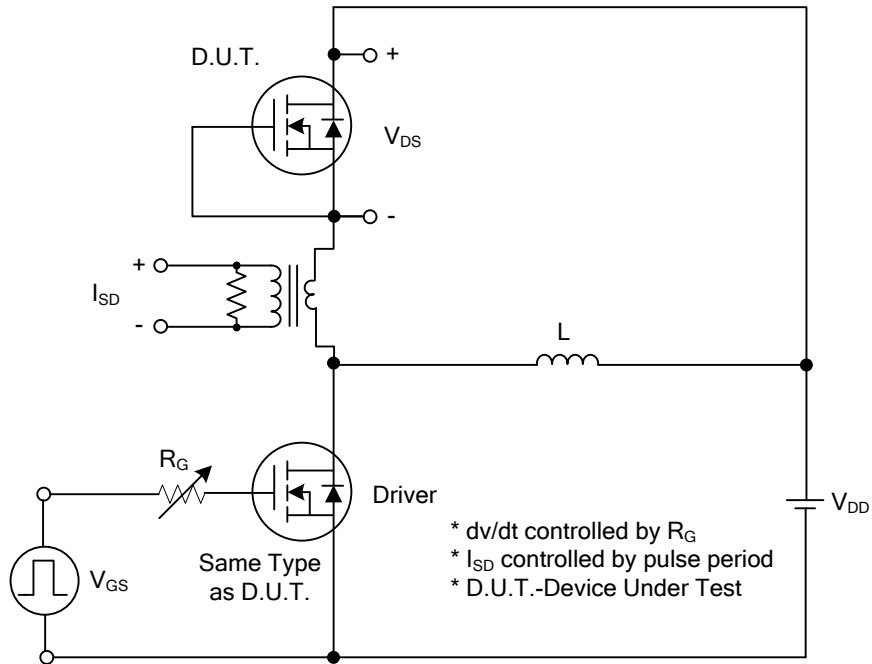
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	Forward $V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
		Reverse $V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		2.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=20\text{A}$			13.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$			22	$\text{m}\Omega$
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		1892		pF
Output Capacitance	C_{OSS}			507		pF
Reverse Transfer Capacitance	C_{RSS}			66		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=80\text{V}$, $V_{GS}=10\text{V}$, $I_D=45\text{A}$		50		nC
Gate to Source Charge	Q_{GS}			8		nC
Gate to Drain Charge	Q_{GD}			13		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=45\text{A}$, $R_G=3\Omega$		10		ns
Rise Time	t_R			17		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			29		ns
Fall-Time	t_F			18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				45	A
Maximum Body-Diode Pulsed Current	I_{SM}				90	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_{SD}=45\text{A}$			1.4	V
Reverse Recovery Time	t_{rr}	$I_F=30\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		44		ns
Reverse Recovery Charge	Q_{rr}				68	

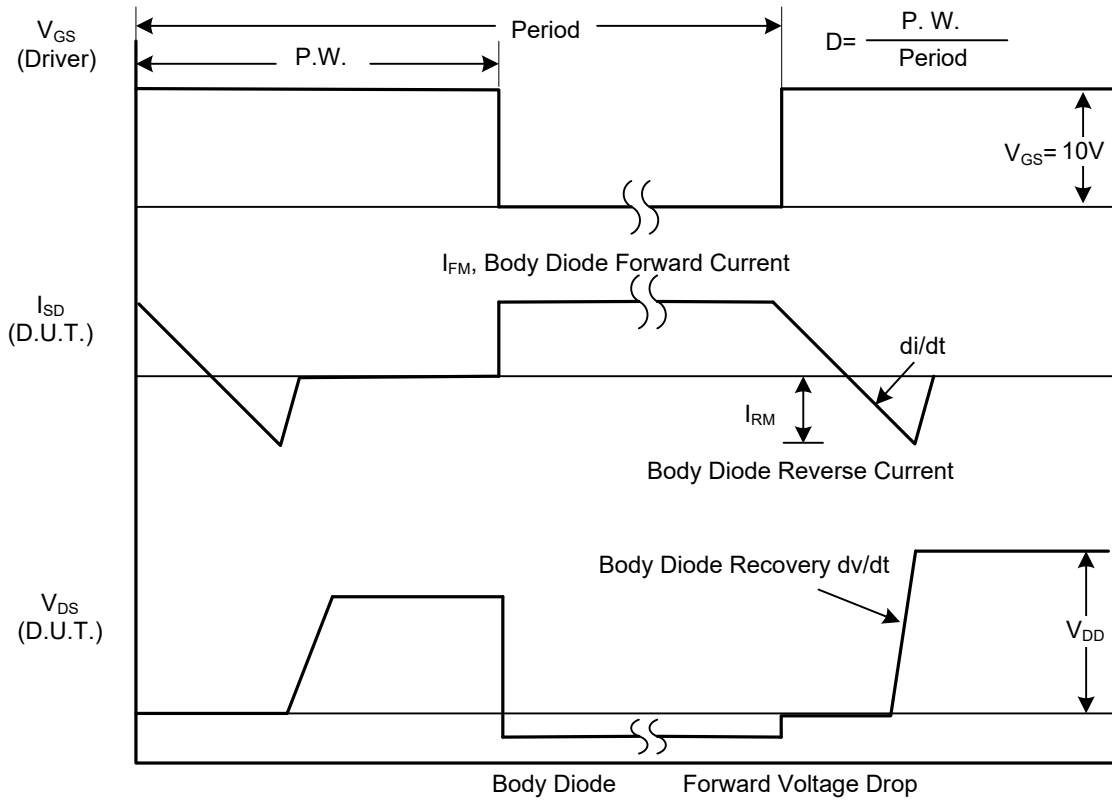
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

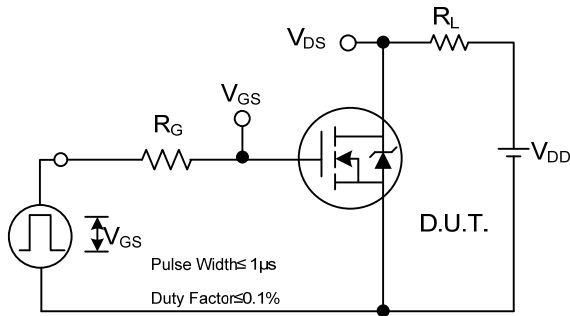


Peak Diode Recovery dv/dt Test Circuit

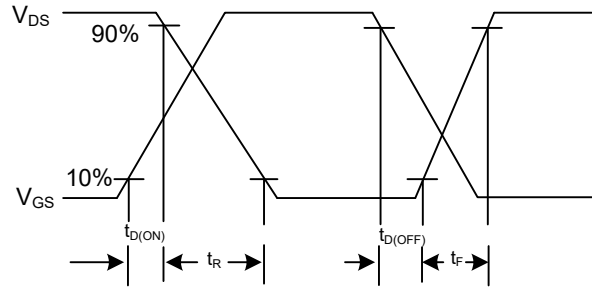


Peak Diode Recovery dv/dt Waveforms

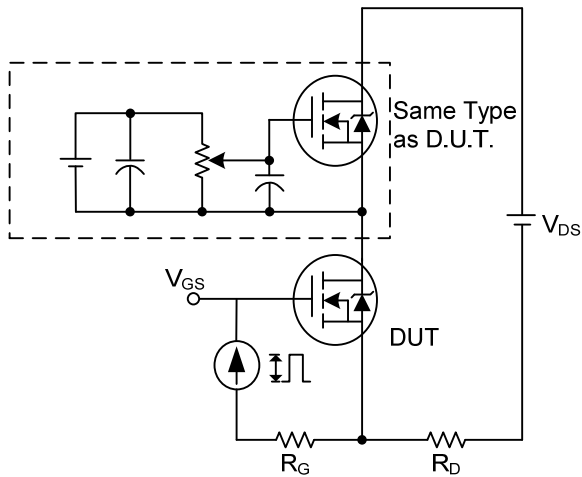
■ TEST CIRCUITS AND WAVEFORMS



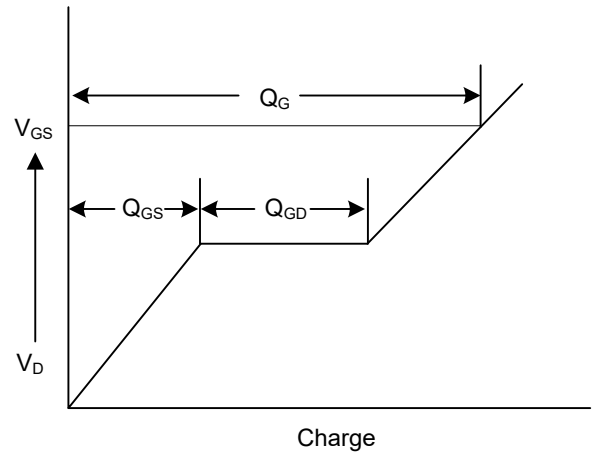
Switching Test Circuit



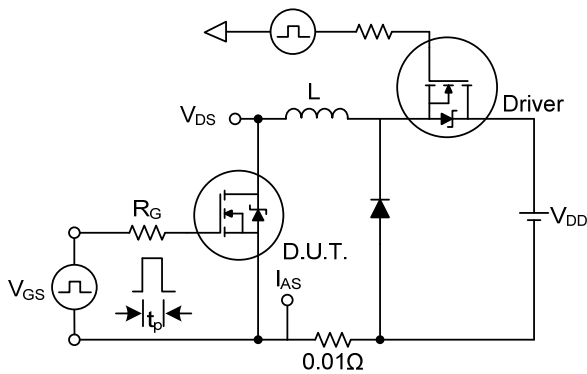
Switching Waveforms



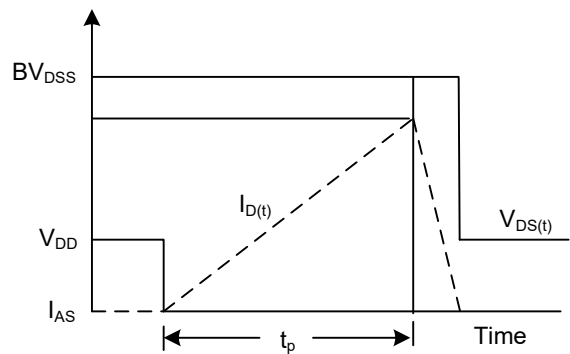
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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