



# 7NM105

*Power MOSFET*

## 7.0A, 1050V N-CHANNEL SUPER-JUNCTION MOSFET

### DESCRIPTION

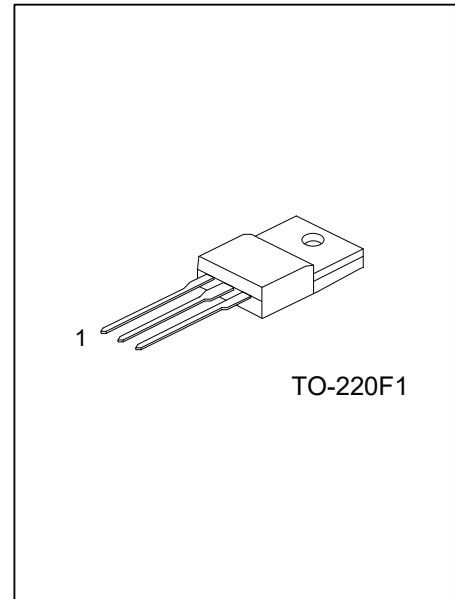
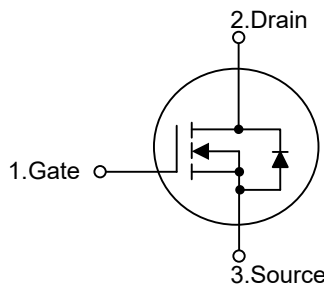
The UTC **7NM105** is an Super Junction MOSFET Structure. It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance.

The UTC **7NM105** is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

### FEATURES

- \*  $R_{DS(ON)} \leq 1.3 \Omega @ V_{GS}=10V, I_D=3.5A$
- \* High switching speed
- \* High breakdown voltage

### SYMBOL



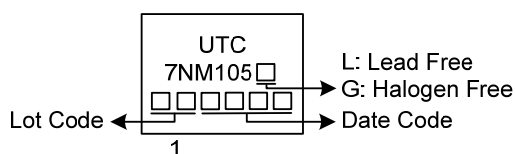
### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7NM105L-TF3-T	7NM105G-TF3-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7NM105G-TF3-T</p> <ul style="list-style-type: none"> <li>(1)Packing Type</li> <li>(2)Package Type</li> <li>(3)Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) T: Tube</li> <li>(2) TF3: TO-220F1</li> <li>(3) G: Halogen Free and Lead Free L: Lead Free</li> </ul>
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### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	1050	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	7	A
	Pulsed	$I_{DM}$	21	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	200	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.6	V/ns
Power Dissipation		$P_D$	27	W
Junction Temperature		$T_J$	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature Range		$T_{STG}$	$-55 \sim +150$	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3.  $L = 100\text{mH}$ ,  $I_{AS} = 2.0\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$  Starting  $T_J = 25^\circ\text{C}$
4.  $I_{SD} \leq 7.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	4.62	$^\circ\text{C}/\text{W}$

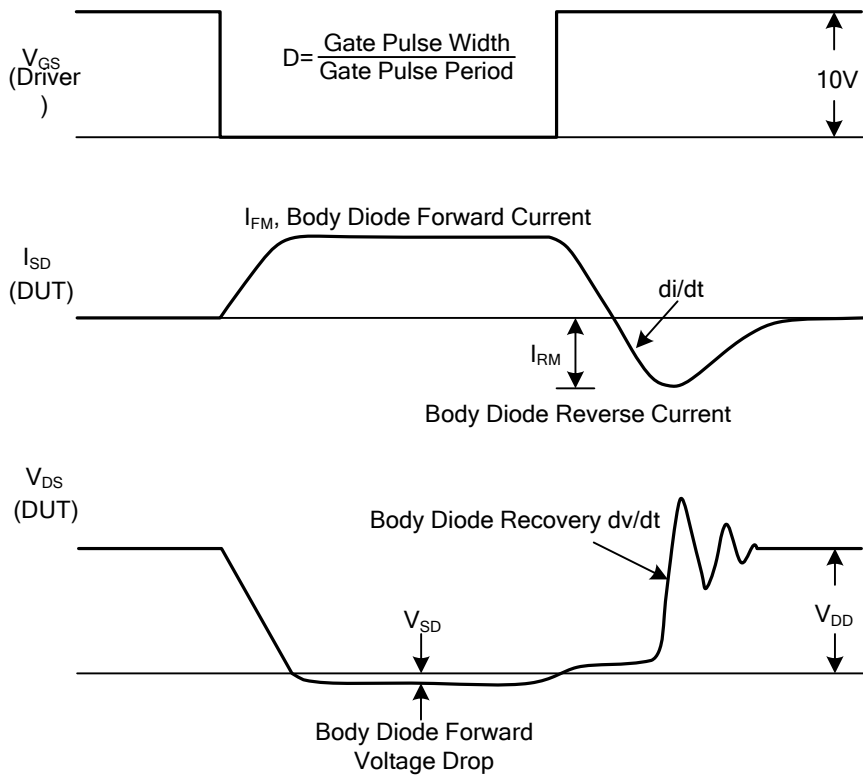
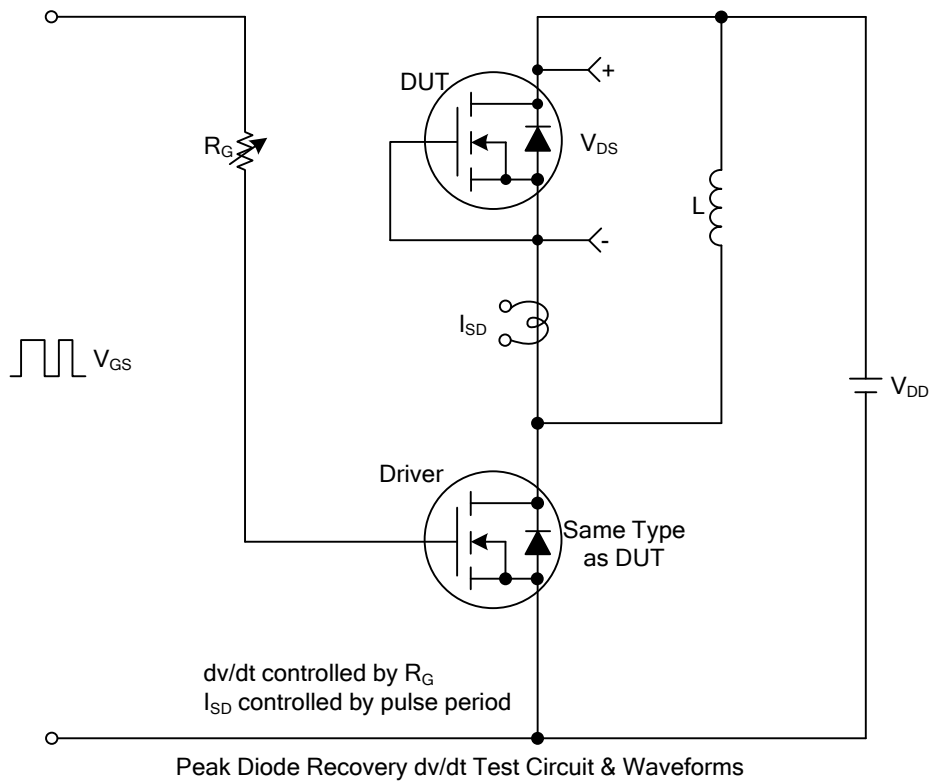
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=0.25\text{mA}$ , $V_{GS}=0\text{V}$	1050			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=1050\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$I_{GSS}$			+100	nA
					Reverse	-100
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$		1.1	1.3	$\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=50\text{V}$ , $f=1.0\text{MHz}$		650		pF
Output Capacitance	$C_{OSS}$			47		pF
Reverse Transfer Capacitance	$C_{RSS}$			3		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{DS}=840\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=7.0\text{A}$ , (Note 1,2)		40		nC
Gate to Source Charge	$Q_{GS}$			10		nC
Gate to Drain Charge	$Q_{GD}$			15		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=100\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=7.0\text{A}$ , $R_G=25\Omega$ (Note 1,2)		7		ns
Rise Time	$t_R$			16.5		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			28		ns
Fall-Time	$t_F$			20		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				7	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				21	A
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_F=7.0\text{A}$ , $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time	$t_{rr}$	$I_S=7.0\text{A}$ , $V_{GS}=0\text{V}$ ,		516		ns
Reverse Recovery Charge	$Q_{rr}$	$dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		6.6		$\mu\text{C}$

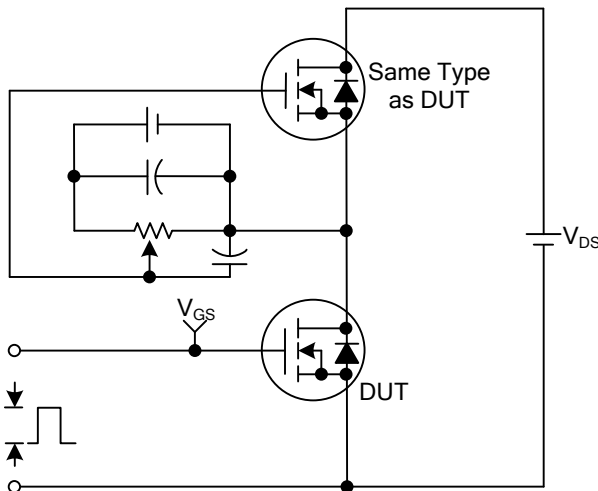
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

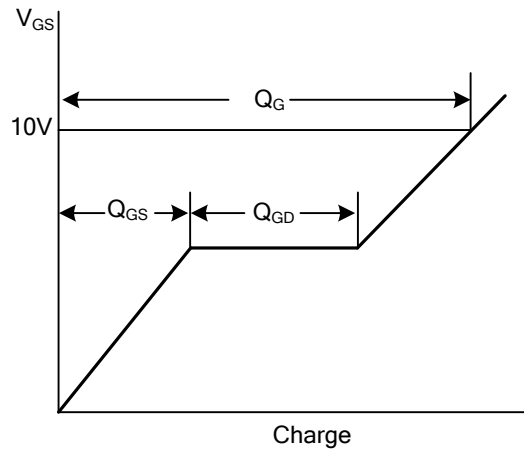
■ TEST CIRCUITS AND WAVEFORMS



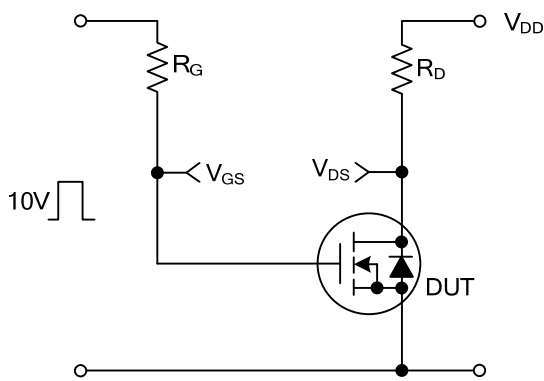
## ■ TEST CIRCUITS AND WAVEFORMS



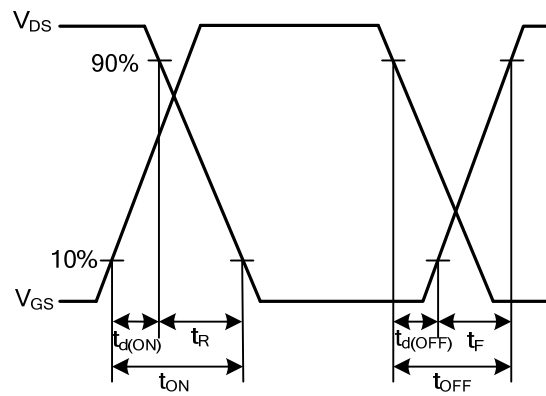
**Gate Charge Test Circuit**



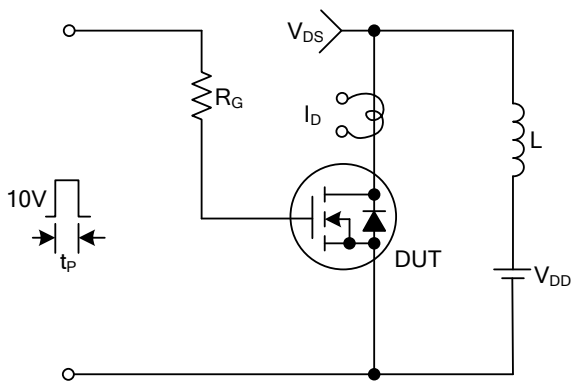
**Gate Charge Waveforms**



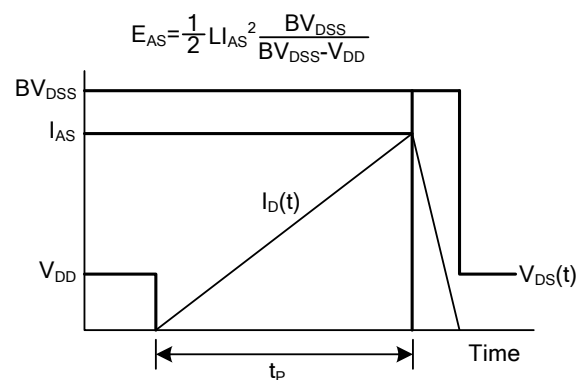
**Resistive Switching Test Circuit**



**Resistive Switching Waveforms**

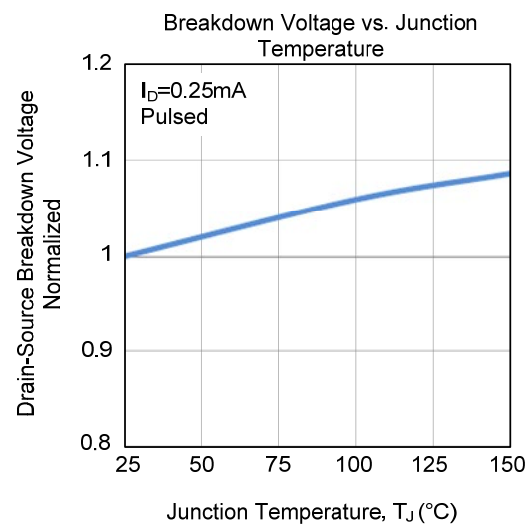
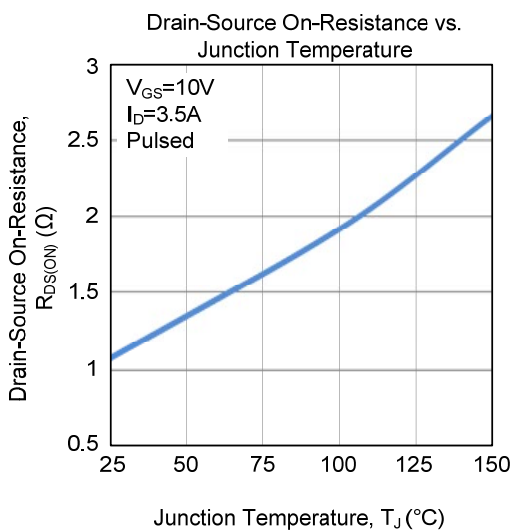
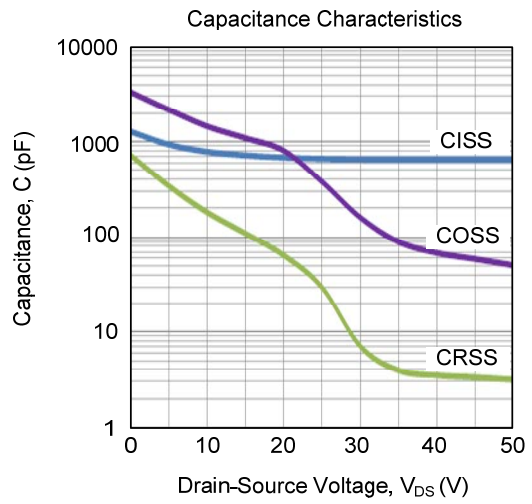
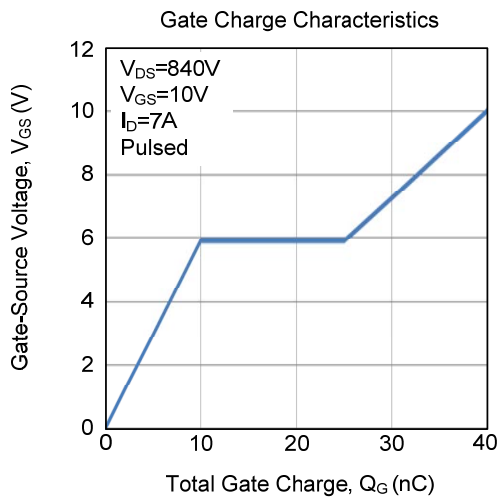
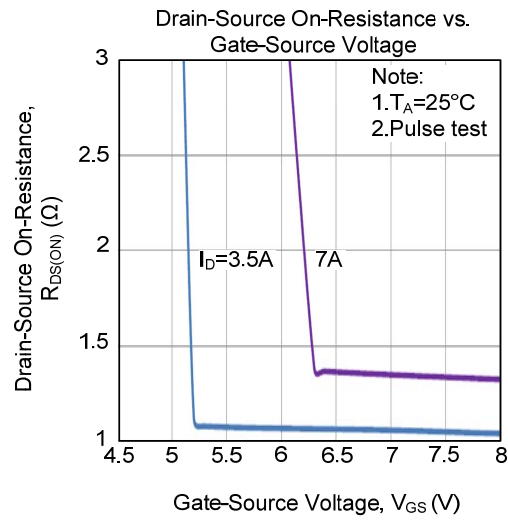
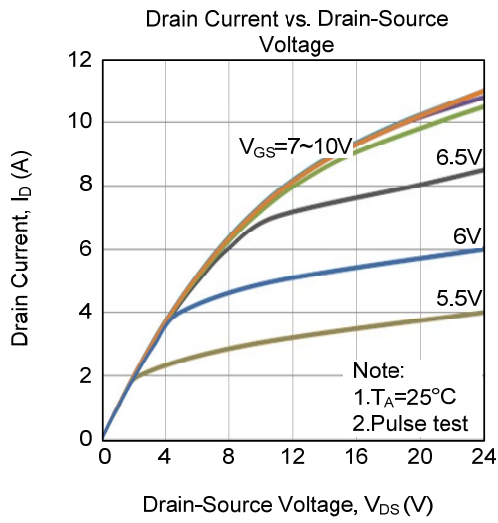


**Unclamped Inductive Switching Test Circuit**

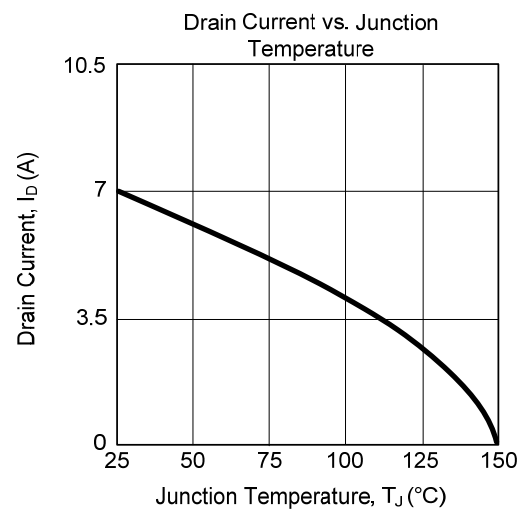
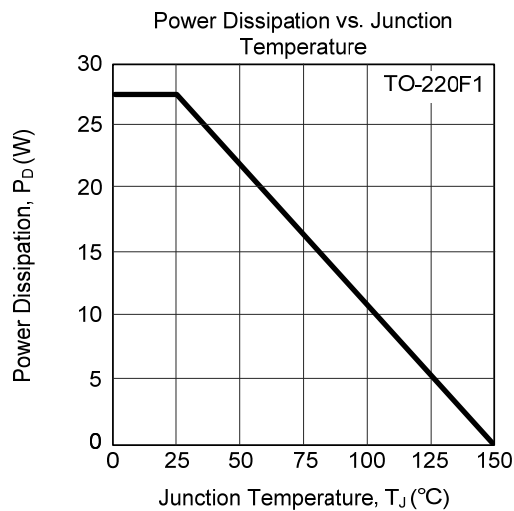
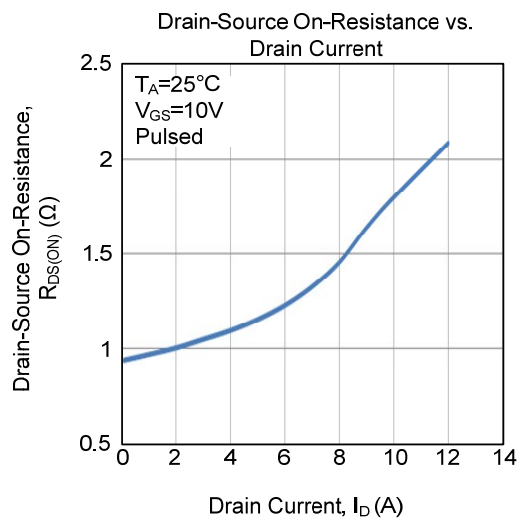
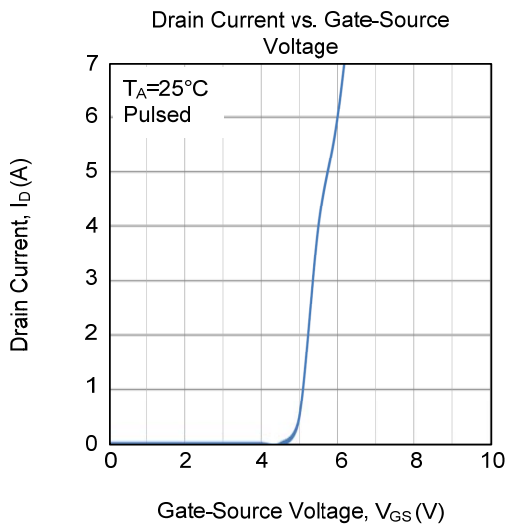
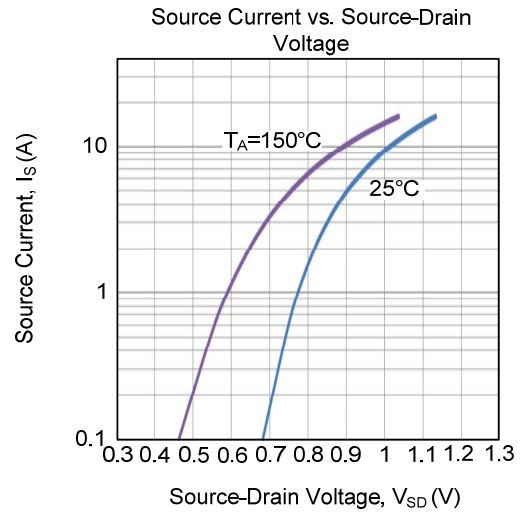
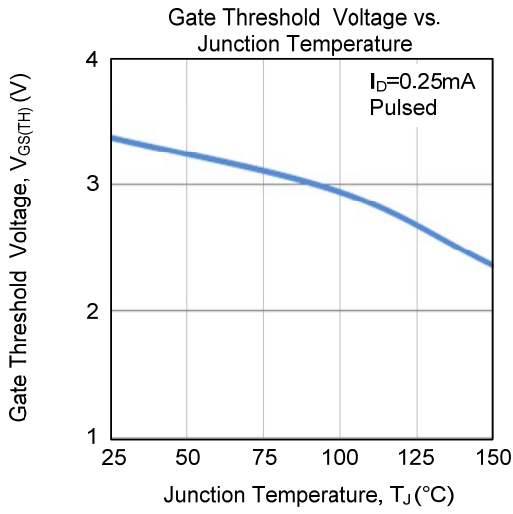


**Unclamped Inductive Switching Waveforms**

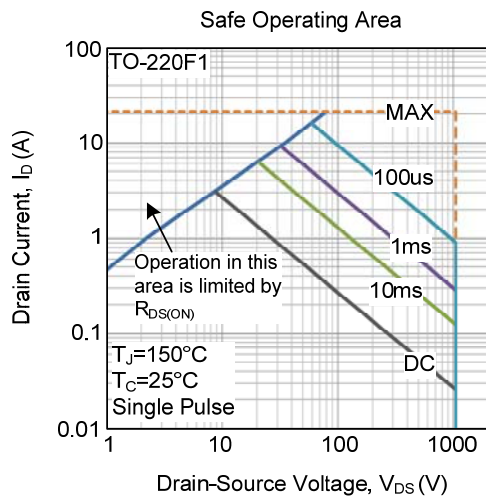
## TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



## ■ TYPICAL CHARACTERISTICS (Cont.)



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