



UCD45360B

Preliminary

CMOS IC

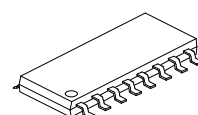
CMOS OSCILLATOR WITH 14-STAGE DIVIDER AND ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

■ DESCRIPTION

The **UCD45360B** consists of an oscillator section with 14 stage Divider, and digitally controlled analog switches.

The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock (C_{IN}) input increments the counter. A high level at the clear (RST) input disables the oscillator ($\overline{CO}$ goes high and CO goes low) and resets the counter to zero (all Q outputs low).

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e. V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low "on" resistance and low "off" leakages. In addition, all three devices have an enable control which, when high, disables all switches to their "off" state.



SOP-16

■ FEATURES

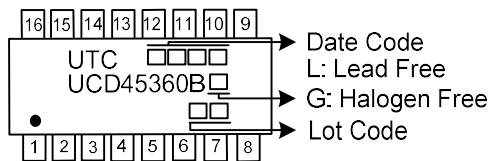
- * Operation Control Voltage: $V_{CC} - GND = 3V$ to $18V$
- * Switch Voltage: $V_{CC} - V_{EE} = 0V$ to $18V$
- * RC or crystal oscillator configuration
- * Low "On" Resistance
- * Low Crosstalk between Switches
- * Fast Switching and Propagation Speeds
- * Wide Operating Temperature Range = $-40^{\circ}C$ to $+125^{\circ}C$

■ ORDERING INFORMATION

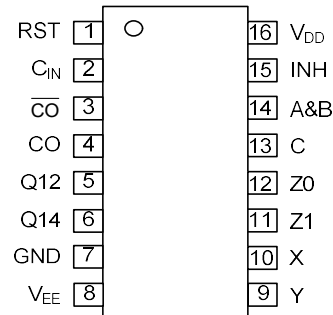
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD45360BL-S16-R	UCD45360BG-S16-R	SOP-16	Tape Reel

UCD45360BG-S16-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



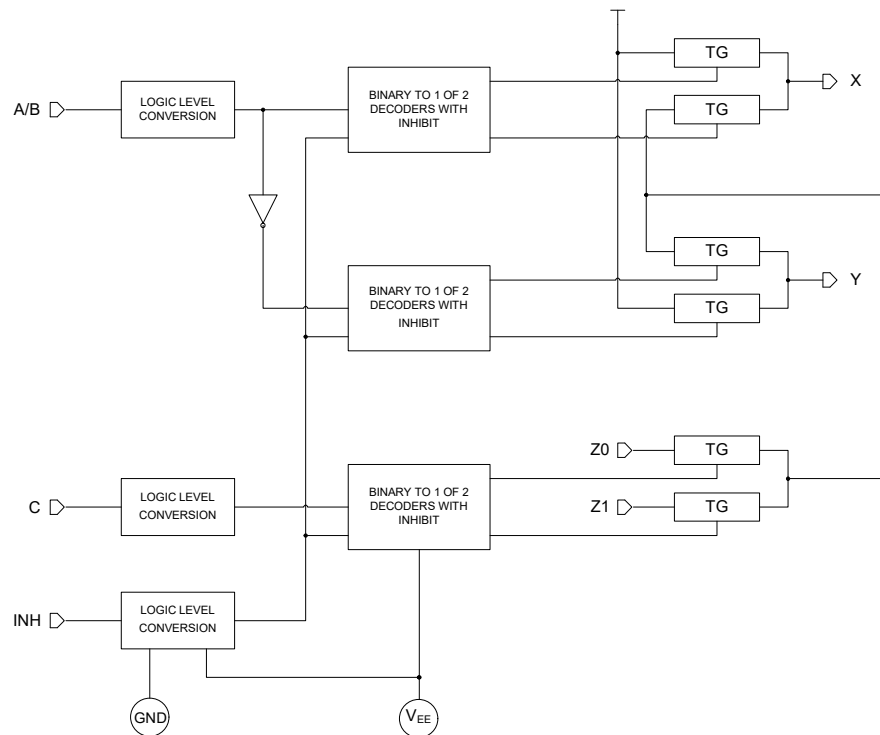
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	RST	Master reset input (active HIGH)
2	C _{IN}	Clock input /oscillator pin
3	CO	External resistor connection
4	CO	External capacitor connection
5	Q12	Counter output
6	Q14	Counter output
7	GND	Ground (0V)
8	V _{EE}	Negative supply voltage
9	Y	Common output
10	X	Common output
11	Z1	Independent input
12	Z0	Independent input
13	C	Select input
14	A&B	Select input
15	INH	Enable input (active LOW)
16	V _{DD}	Positive supply power

The logic diagram illustrates a 14-bit shift register with parallel load and ripple-carry adder. The register consists of 14 flip-flops (FF1 to FF14) with inputs Φ and $\bar{\Phi}$, and outputs Q and $\bar{Q}$. The $\bar{Q}$ outputs of FF12 and FF14 are inverted to produce Q_{12} and Q_{14} . The parallel load is controlled by a RST signal, which is inverted and connected to the $\bar{\Phi}$ inputs of all flip-flops. The data for parallel load is provided by C_{IN} and CO signals. The ripple-carry adder is implemented using a chain of XOR gates. The first XOR gate takes C_{IN} and the $\bar{Q}$ output of FF1 as inputs. The output of this gate is connected to the $\bar{\Phi}$ input of FF2. Subsequent XOR gates take the $\bar{Q}$ output of the previous flip-flop and the CO signal as inputs, with the output of each gate connected to the $\bar{\Phi}$ input of the next flip-flop. The final output of the adder is the $\bar{Q}$ output of FF14, which is inverted to produce Q_{14} .



■ ABSOLUTE MAXIMUM RATING (T_A = 25°C, unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Range	V _{CC} - GND	-0.5 ~ 20	V
	V _{CC} - V _{EE}	-0.5 ~ 20	V
Input Voltage Range (Note 2)	V _{IN} - GND	-0.5 ~ 20	V
	V _{IN} - V _{EE}	-0.5 ~ 20	V
Input Current	I _I	±10	mA
DC switch Current	I _O	±25	mA
Total Power Dissipation	P _D	500	mW
Storage Temperature	T _{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	110	°C/W

■ RECOMMENDED OPERATING CONDITIONS (NOTE)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{DD}		3		18	V
Input-Pulse Width	t _W	V _{DD} =5V	100			ns
		V _{DD} =10V	40			ns
		V _{DD} =15V	30			ns
Reset Pulse Width	t _W	V _{DD} =5V	120			ns
		V _{DD} =10V	60			ns
		V _{DD} =15V	40			ns
Input-Pulse Frequency	F _{CIN}	V _{DD} =5V			3.5	MHz
		V _{DD} =10V			8	MHz
		V _{DD} =15V			12	MHz
Operating Temperature	T _A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ **STATIC ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Device Current	I_{DD}	$V_{DD}=5\text{V}$			5	μA
		$V_{DD}=10\text{V}$			10	μA
		$V_{DD}=15\text{V}$			20	μA
		$V_{DD}=20\text{V}$			100	μA
Low Level Input Voltage	V_{IL}	$V_{DD}=5\text{V}$			1.5	V
		$V_{DD}=10\text{V}$			3	V
		$V_{DD}=15\text{V}$			4	V
High Level Input Voltage	V_{IH}	$V_{DD}=5\text{V}$	3.5			V
		$V_{DD}=10\text{V}$	7			V
		$V_{DD}=15\text{V}$	11			V
Low Level Output Voltage (Q12/Q14)	V_{OL}	$V_{DD}=5\text{V}$			0.05	V
		$V_{DD}=10\text{V}$			0.05	V
		$V_{DD}=15\text{V}$			0.05	V
High Level Output Voltage (Q12/Q14)	V_{OH}	$V_{DD}=5\text{V}$	4.95			V
		$V_{DD}=10\text{V}$	9.95			V
		$V_{DD}=15\text{V}$	14.95			V
Low Level Output Current (Q12/Q14)	I_{OL}	$V_{DD}=5\text{V}, V_{OL}=0.4\text{V}$	0.51			mA
		$V_{DD}=10\text{V}, V_{OL}=0.5\text{V}$	1.3			mA
		$V_{DD}=15\text{V}, V_{OL}=1.5\text{V}$	3.4			mA
High Level Output Current (Q12/Q14)	I_{OH}	$V_{DD}=5\text{V}, V_{OH}=2.5\text{V}$	-1.6			mA
		$V_{DD}=5\text{V}, V_{OH}=4.6\text{V}$	-0.51			mA
		$V_{DD}=10\text{V}, V_{OH}=9.5\text{V}$	-1.3			mA
		$V_{DD}=15\text{V}, V_{OH}=13.5\text{V}$	-3.4			mA
Input Current	I_{IN}	$V_{DD}=18\text{V}, V_{IN}=0 \text{ or } 18\text{V}$			± 0.1	μA
OFF Channel Leakage Current	I_{LEAK}	$V_{DD}=18\text{V}$			± 100	nA
Drain to Source ON Resistance	$R_{DS(ON)}$	$V_{DD}=5\text{V}$			1050	Ω
		$V_{DD}=10\text{V}$			400	Ω
		$V_{DD}=15\text{V}$			240	Ω
Low Level Output Current (CO)	I_{OL}	$V_{DD}=5\text{V}, V_{OL}=0.4\text{V}$	0.16			mA
		$V_{DD}=10\text{V}, V_{OL}=0.5\text{V}$	0.42			mA
		$V_{DD}=15\text{V}, V_{OL}=1.5\text{V}$	1			mA
High Level Output Current (CO)	I_{OH}	$V_{DD}=5\text{V}, V_{OH}=4.6\text{V}$	-0.16			mA
		$V_{DD}=10\text{V}, V_{OH}=9.5\text{V}$	-0.42			mA
		$V_{DD}=15\text{V}, V_{OH}=13.5\text{V}$	-1			mA

■ **DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$, $t_R, t_F = 20\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time Address-to-Signal OUT (Channels ON or OFF)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$ $R_L = 10\text{k}\Omega$	$V_{DD} = 5\text{V}$		720	ns
			$V_{DD} = 10\text{V}$		320	ns
			$V_{DD} = 15\text{V}$		240	ns
Propagation Delay Time (Signal Input to Output)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$ $R_L = 200\text{k}\Omega$	$V_{DD} = 5\text{V}$		60	ns
			$V_{DD} = 10\text{V}$		30	ns
			$V_{DD} = 15\text{V}$		20	ns

■ **SWITCHING CHARACTERISTICS** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator Frequency	f_{OSC}	$C_X = 150\text{pF}$ $R_S = 10\text{M}\Omega$ $R_X = 3.3\text{M}\Omega$	$V_{DD} = 2\text{V}$	560		Hz
			$V_{DD} = 7\text{V}$	610		Hz
Variation of Frequency (Unit to Unit)		$C_X = 200\text{pF}$ $R_S = 560\text{k}\Omega$ $R_X = 50\text{k}\Omega$	$V_{DD} = 5\text{V}$	$23 \pm 10\%$		kHz
			$V_{DD} = 10\text{V}$	$24 \pm 10\%$		kHz
			$V_{DD} = 15\text{V}$	$25 \pm 10\%$		kHz
Variation of Frequency with voltage change (Same Unit)		$C_X = 200\text{pF}$ $R_S = 560\text{k}\Omega$ $R_X = 50\text{k}\Omega$	$V_{DD} = 5\text{V}$ to 10V	1.5		kHz
			$V_{DD} = 10\text{V}$ to 15V	0.5		kHz
Rx Max.		$V_{DD} = 5\text{V}$, $C_X = 10\mu\text{F}$			20	$\text{M}\Omega$
		$V_{DD} = 10\text{V}$, $C_X = 50\mu\text{F}$			20	$\text{M}\Omega$
		$V_{DD} = 15\text{V}$, $C_X = 10\mu\text{F}$			10	$\text{M}\Omega$
Cx Max.		$V_{DD} = 5\text{V}$, $R_X = 500\text{k}\Omega$			1000	μF
		$V_{DD} = 10\text{V}$, $R_X = 300\text{k}\Omega$			50	μF
		$V_{DD} = 15\text{V}$, $R_X = 300\text{k}\Omega$			50	μF
Max. C_{IN} Input Pulse Frequency		$V_{DD} = 5\text{V}$	3.5			MHz
		$V_{DD} = 10\text{V}$	8			MHz
		$V_{DD} = 15\text{V}$	12			MHz
Min. C_{IN} Input Pulse Width	t_W	$V_{DD} = 5\text{V}$			100	ns
		$V_{DD} = 10\text{V}$			40	ns
		$V_{DD} = 15\text{V}$			30	ns
Min. Reset Pulse Width	t_W	$V_{DD} = 5\text{V}$			120	ns
		$V_{DD} = 10\text{V}$			60	ns
		$V_{DD} = 15\text{V}$			40	ns
RST Propagation Delay Time	t_{PHL}	$V_{DD} = 5\text{V}$			360	ns
		$V_{DD} = 10\text{V}$			160	ns
		$V_{DD} = 15\text{V}$			100	ns

TYPICAL APPLICATION CIRCUIT

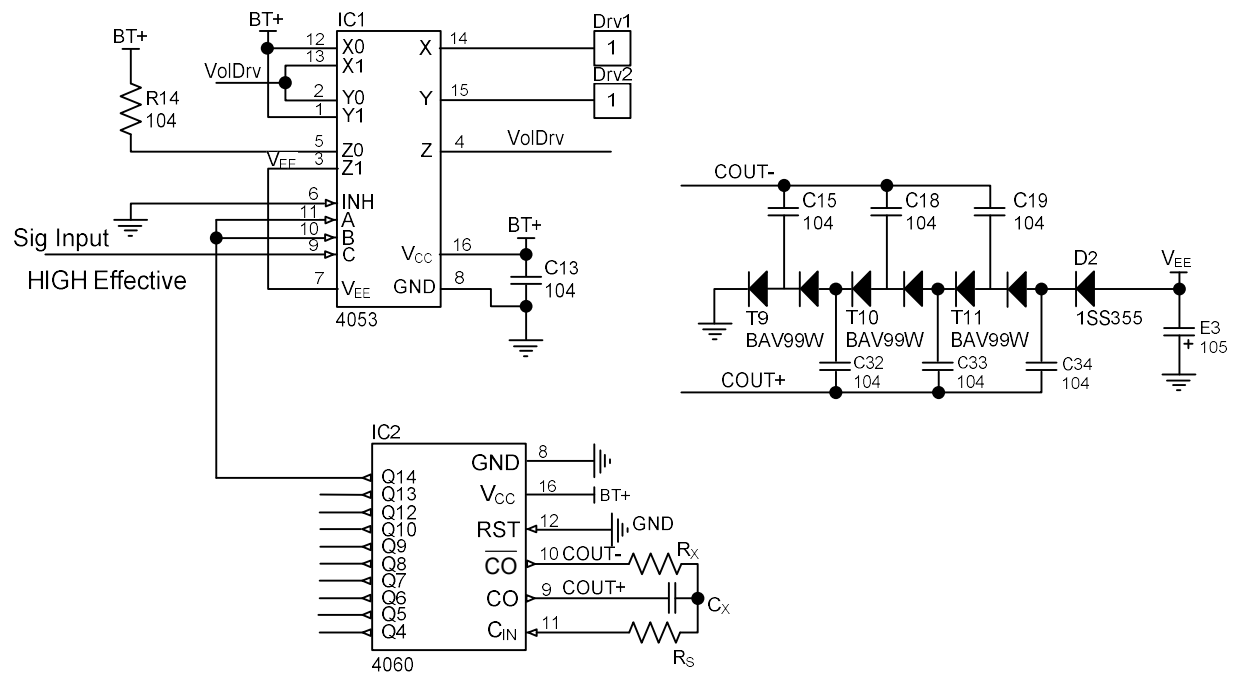


Figure 1. Basic Working Circuit Principle

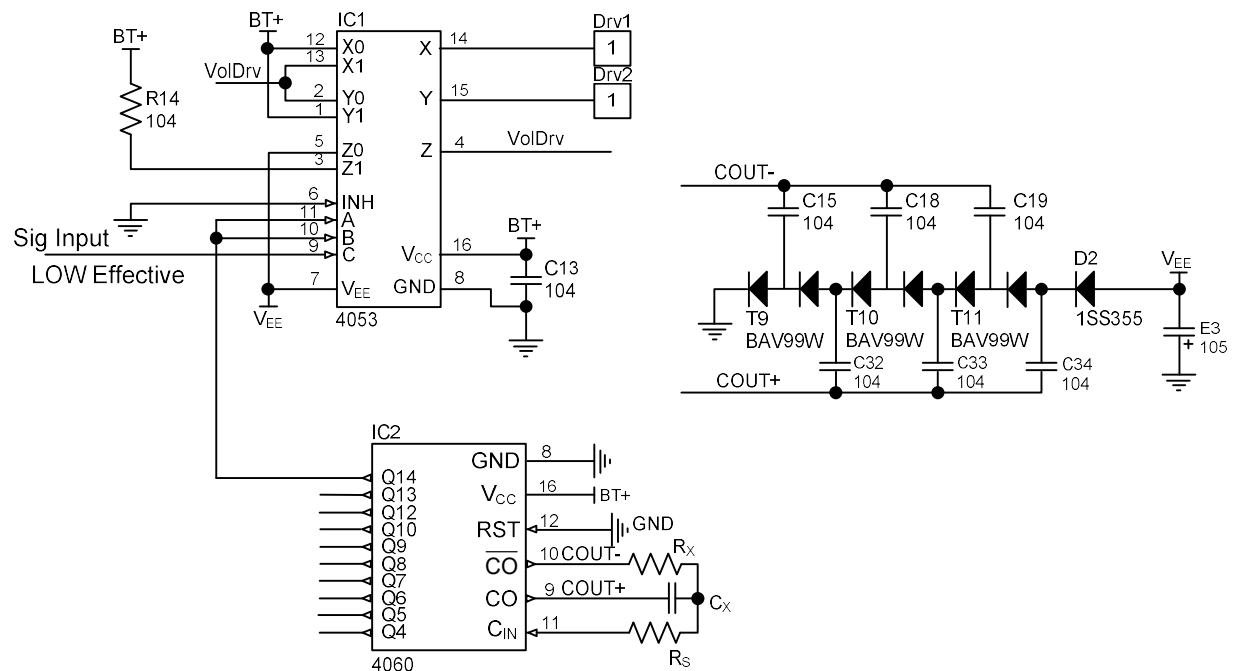


Figure 2. Basic Working Circuit Principle

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