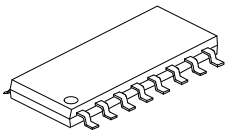
UCL1099

BCD IC

HALF-BRIDGE LLC RESONANT CONTROLLER



SOP-16

■ DESCRIPTION

The UTC **UCL1099** is a high-performance enhanced half-bridge LLC resonant controller IC with high integration, high efficiency and outstanding reliability.

The UTC **UCL1099** regulates the output voltage by adjusting the system operating frequency, and the operating frequency range can be configured via external peripheral components connected to dedicated pins. The device outputs two gate drive signals. The high-side and low-side power switches turn on/off with a 180° phase shift within one switching cycle. A fixed dead time is inserted between the two non-overlapping drive signals to guarantee soft-switching operation and superior high-frequency performance of the power system.

An integrated soft-start circuit is implemented inside the chip. Upon power-up, the system starts at the pre-defined maximum switching frequency, then the operating frequency gradually decreases until the control loop takes over regulation. This mechanism effectively suppresses output voltage overshoot. The soft-start duration is configurable through external peripheral components on the corresponding pin.

A high-side bootstrap charging diode with an equivalent series resistance of 100 Ω is integrated on-chip to simplify system implementation. At light-load conditions, the controller operates in Burst mode to significantly cut switching losses and boost light-load efficiency.

The UTC **UCL1099** integrates comprehensive control and protection functions, including brown-in/brown-out (BIBO) line voltage protection, two-stage overcurrent protection (OCP and AOCP), over-temperature protection (OTP), as well as low-side and high-side under-voltage lockout protection (UVLO_LS, UVLO_HS).

Additionally, the chip incorporates an interface for communication with the PFC controller. It can rapidly disable the PFC stage when abnormal operating conditions are detected, such as OCP triggering, the DIS pin being pulled high, or operation under Burst mode.

■ FEATURES

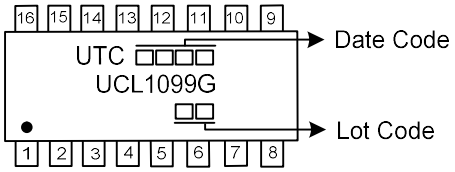
* 700V high-side gate driver
* Integrated bootstrap charging diode
* 1.5A/2A source/sink capability for both high-side and low-side gate drivers
* Maximum operating frequency up to 600 kHz
* PFC interface
* Burst-mode operation at light-load
* Two-stage overcurrent protection with programmable OCP delay time
* Current hysteresis BIBO protection
* Programmable soft-start function
* Green & Pb Free

■ ORDERING INFORMATION

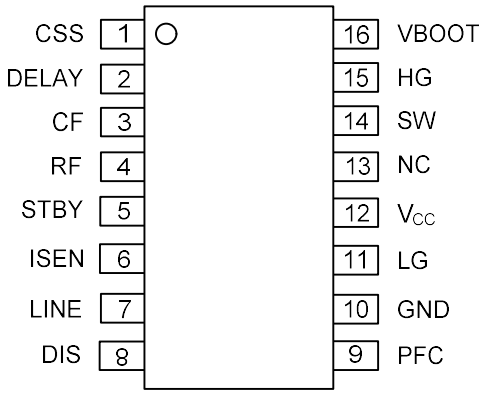
Ordering Number	Package	Packing
UCL1099G-S16-R	SOP-16	Tape Reel

UCL1099G-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free

■ MARKING



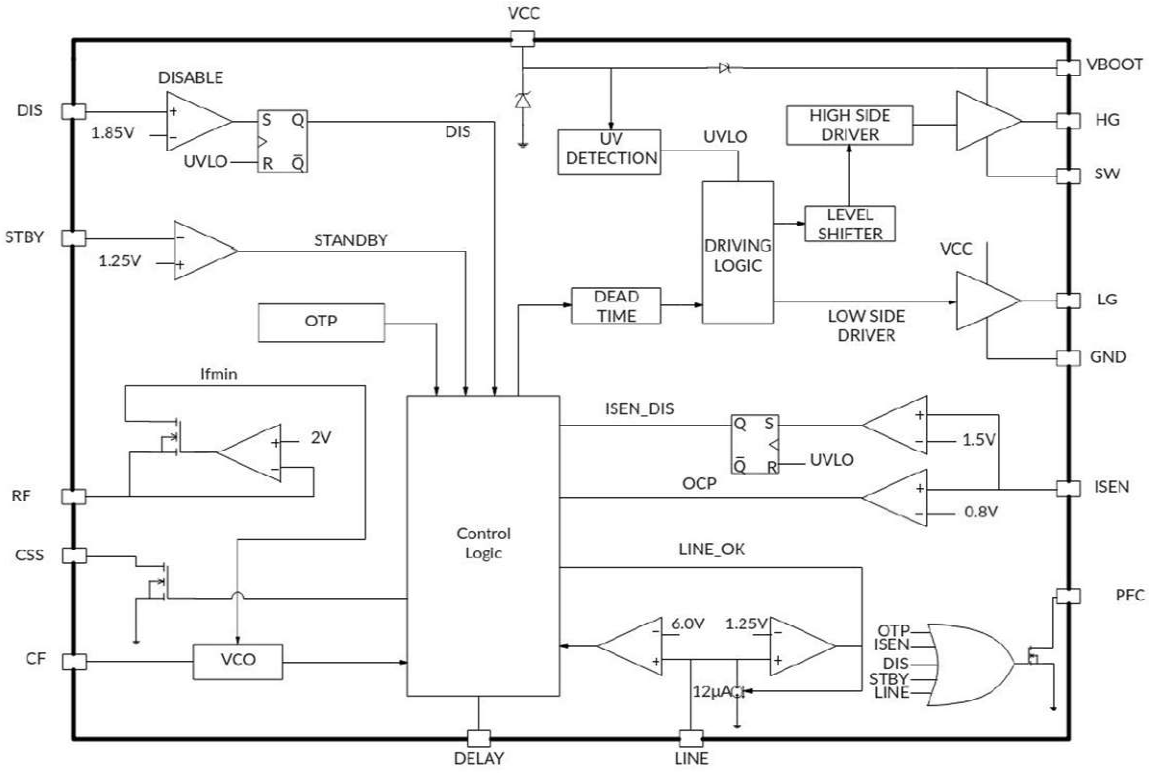
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	CSS	Soft-start
2	DELAY	Over-current delay shutdown
3	CF	Time-set
4	RF	Switching frequency set
5	STBY	Burst-mode control
6	ISEN	Current sense
7	LINE	Line voltage sense
8	DIS	Latch pin. Short to GND if unused
9	VBOOT	High-side floating supply
10	HG	High-side gate driver
11	SW	High-side switching source
12	NC	No connection
13	V_{CC}	IC supply voltage
14	LG	Low-side gate driver
15	GND	IC Ground
16	PFC	Interface to PFC

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
High-Side Floating Supply Voltage	V_{BOOT}		-0.3 ~ 700	V
High-Side Floating Ground Voltage	V_{SW}		-3 ~ V_{BOOT}-18	V
Maximum V_{SW} Slew Rate	dV_{SW}/dt		50	V/ns
Supply Voltage	V_{CC}	I_{CC} ≤ 25mA	-0.3 ~ 16.0	V
Maximum Voltage	V_{PFC}	Pin floating	-0.3 ~ V_{CC}	V
Maximum Current	I_{RF}		2.0	mA
Low-Side Gate Driver Voltage	LG		-0.3 ~ 16.0	V
Analog Inputs and Outputs Voltage	V_A		-0.3 ~ 6.0	V
Human Body Model	ESD	Pin14, Pin15, Pin16	±1.2	kV
		Other pins	±2.0	kV
Continuous Power Dissipation (T_A=25°C)	P_D		1.56	W
Junction Temperature	T_J		-40 ~ 150	°C
Lead Temperature(Solder)	T_L		260	°C
Storage Temperature	T_{STG}		-55 ~ 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{CC} Operating Range	V_{CC}		8.9		15.5	V
IC Switch-ON Threshold	V_{CC_ON}	Rising Edge	10.2	10.9	11.6	V
IC Switch-OFF Threshold	V_{CC_OFF}	Falling Edge	7.1	7.8	8.5	V
Hysteresis	V_{Hys}			3.1		V
V_{CC} Clamp Voltage	V_{Clamp}		15.5	16.3	17.1	V
SUPPLY CURRENT						
Start-up Current	I_{Start_up}	V_{CC} = V_{CC_On}-0.2V		270	320	μA
Quiescent Current	I_Q	Normal operation, V_{STBY} = 1V		1.5	2	mA
Operating Current	I_{OD}	Normal operation, V_{STBY} = V_{RF}		3.5	5	mA
Residual Consumption	I_{RES}	V_{DIS} > 1.85 V or V_{ISEN} > 1.5V or V_{DELAY} > 3.5 V or V_{LINE} < 1.25 V or V_{LINE} > 6V		350	400	μA
HIGH-SIDE FLOATING SUPPLY						
VBOOT Pin Leakage Current	$I_{LKVBOOT}$	V_{BOOT} = 700V			10	μA
SW pin Leakage Current	I_{LKSW}	V_{SW} = 682V			10	μA
Bootstrap Diode Equivalent Resistance	$R_{DIOBOOT}$			80		Ω
OVER-CURRENT COMPARATOR (ISEN)						
Input Bias Current	I_{ISEN}	V_{ISEN} = 0 to V_{TH}			1	μA
Leading Edge Blanking	t_{LEB}			250		ns
Frequency-Shift Threshold	V_{ISENth}		0.75	0.8	0.85	V
Latch-Off Threshold	$V_{ISENlatch}$		1.41	1.5	1.59	V
LINE VOLTAGE SENSING (LINE)						
Threshold Voltage	V_{TH}		1.20	1.25	1.3	V
Current Hysteresis	I_{Hys}	V_{CC} > 5V, V_{LINE} = 1V	10	12	14	μA
Clamp Voltage	V_{Clamp}		5.6	6.0	6.4	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DIS FUNCTION						
Input Bias Current	I_{DIS}				1	μA
Latch Threshold Voltage	V_{TH}		1.75	1.85	1.95	V
OSCILLATOR						
Output Duty Cycle	D	HG and LG	48	50	52	%
Oscillation Frequency	f_{OSC}				600	KHz
Dead-Time	D_T		280	330	380	ns
CF Peak Voltage	V_{CFp}			3.75		V
CF Valley Voltage	V_{CFv}			1.0		V
Voltage Reference at RF Pin	V_{REF}		1.95	2.0	2.05	V
PFC FUNCTION						
Low Saturation Level	V_L	I_{PFC} = 1mA, V_{DIS} = 1.5V			0.2	V
Discharge Resistance	R			120		Ω
SOFT-START FUNCTION (C_{SS})						
Discharge Resistance	R			100		Ω
BURST-MODE CONTROL (STBY)						
Disable Threshold	V_{TH}		1.23	1.28	1.33	V
Hysteresis	V_{Hys}			100		mV
OVER-CURRENT DELAY SHUTDOWN (DELAY)						
Charge Current	I_{DELAY}	V_{DELAY} = 1V, V_{ISEN} = 0.85V	110	130	150	μA
Frequency-Up Threshold	V_{TH1}		1.95	2.0	2.05	V
Shut Down Threshold	V_{TH2}		3.42	3.5	3.58	V
Restart Threshold	V_{TH3}		0.25	0.3	0.35	V
LOW-SIDE GATE DRIVER (LG TO GND)						
Peak Source Current	$I_{Sourcepk}$		1.5			A
Peak Sink Current	I_{Sinkpk}		2.0			A
Source Resistor	R_{Source}			4		Ω
Sink Resistor	R_{Sink}			2		Ω
Rise Time	t_r			20		ns
Fall Time	t_f			20		ns
HIGH-SIDE GATE DRIVER (HG TO SW)						
Peak Source Current	$I_{Sourcepk}$		1.5			A
Peak Sink Current	I_{Sinkpk}		2.0			A
Source On-Resistance	R_{Source}			4		Ω
Sink On-Resistance	R_{Sink}			2		Ω
Rise Time	t_r			20		ns
Fall Time	t_f			20		ns
Bootstrap UVLO Threshold	V_{Bs_Uvlo}			4.5		V
Bootstrap UVLO Recovery Threshold	V_{Bs_Re}			5.5		V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{otp}			150		°C
Thermal Shutdown Recovery Threshold	T_{otp_Re}			120		°C

■ FUNCTION DESCRIPTIONS

Oscillator

The charging and discharging duration of the CF capacitor determines the oscillation frequency. The voltage across the CF capacitor swings between the peak level (VCFp) and valley level (VCFv) to generate a triangular waveform, as illustrated in Figure 1.

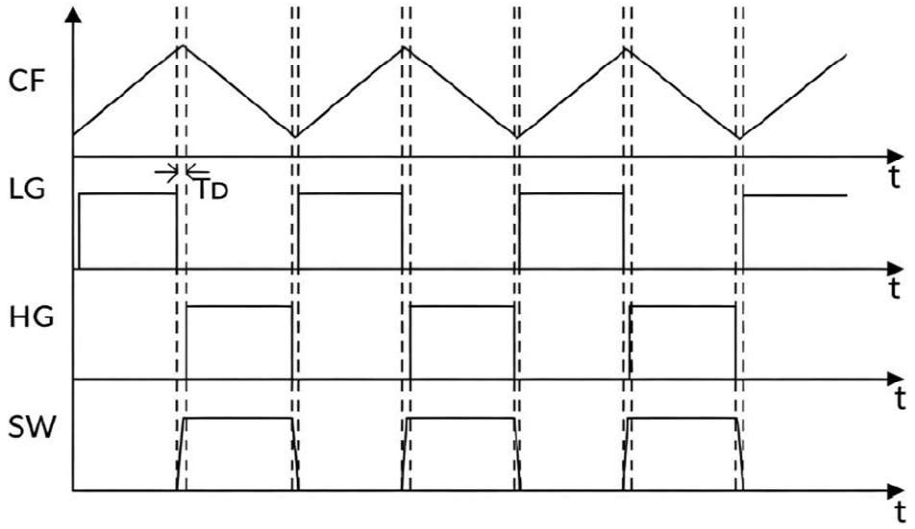


Figure 1. CF Oscillation Waveform and Output Drive Signals

The network connected to the RF pin regulates the charging and discharging current of the CF capacitor, as shown in Figure 2. The current source of the RF pin charges the CF capacitor via Current Source 1 (IS-1). At the start of each switching cycle, IS-1 charges the CF capacitor until its voltage reaches the peak threshold. Afterwards, the discharge current source (IS-2), which outputs twice the current of the RF pin current source, is activated to discharge the CF capacitor at a current equal to the RF pin current. Once the CF capacitor voltage drops to the valley threshold, IS-2 turns off and a new switching cycle initiates.

The network connected to the RF pin is described below with reference to Figure 2.

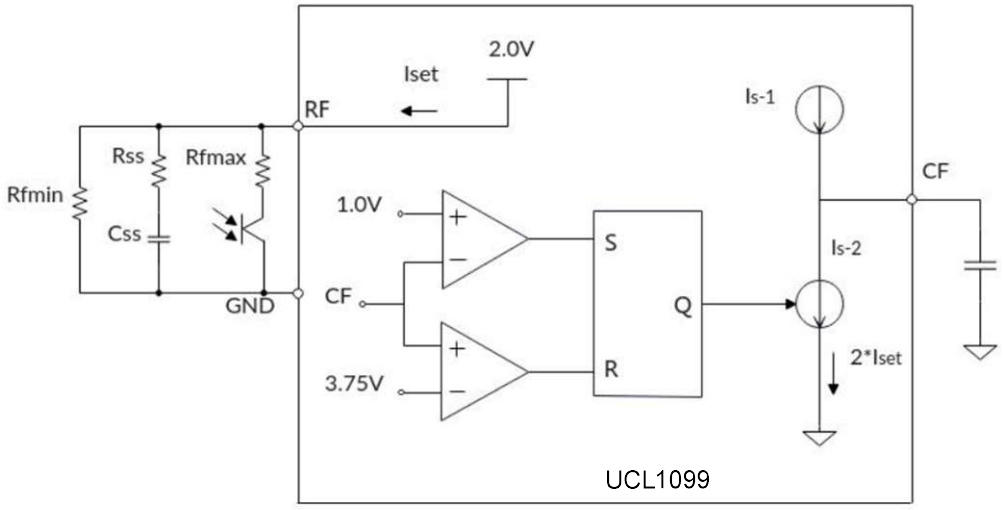


Figure 2. Block Diagram of Oscillator Module

■ FUNCTION DESCRIPTIONS (Cont.)

The minimum switching frequency fmin is determined by the resistor Rfmin connected between the RF pin and GND.

During normal operation, the circuit modulates the switching frequency by adjusting the current flowing through resistor Rfmax via an optocoupler. The magnitude of this current reflects the output voltage level, realizing closed-loop regulation of the output voltage. When the optocoupler enters saturation and the current through Rfmax reaches its maximum value, the system operates at the preset maximum frequency fmax.

The RC network between RF and GND defines the frequency characteristic during system soft-start (refer to the Soft-Start section for details).

The calculation formulas(1) for fmin and fmax are given as follows:

$$\begin{aligned} fmin &= \frac{1}{3 \times CF \times RFmin} \\ fmax &= \frac{1}{3 \times CF \times (RFmin \| RFmax)} \end{aligned} \quad (1)$$

Burst Mode Operation at Light Load

Under light-load or no-load conditions, the switching frequency of the resonant half-bridge is clamped to the preset maximum frequency fmax. To achieve precise output voltage regulation and reduce power consumption, the UTC **UCL1099** incorporates dedicated light-load Burst mode. This mode drastically cuts the average switching frequency (typically by 50%–70%) and effectively suppresses average residual magnetizing current and associated power losses.

Burst mode is enabled via configuration of the STBY pin of the UTC **UCL1099**: when the voltage of this pin falls below V_{TH}, the IC disables the high-side and low-side gate drive outputs (HG/LG). Only the 2V reference voltage (V_{REF}) on the RF pin and soft-start (CSS) pin is retained, minimizing the chip's internal power dissipation. Once the STBY pin voltage rises back to V_{TH} + 100 mV, the system resumes normal operating mode.

Based on the operating principle of Burst mode, the STBY pin voltage must be tied into the feedback loop. Connect the STBY pin to the optocoupler feedback signal as shown in Figure 3.

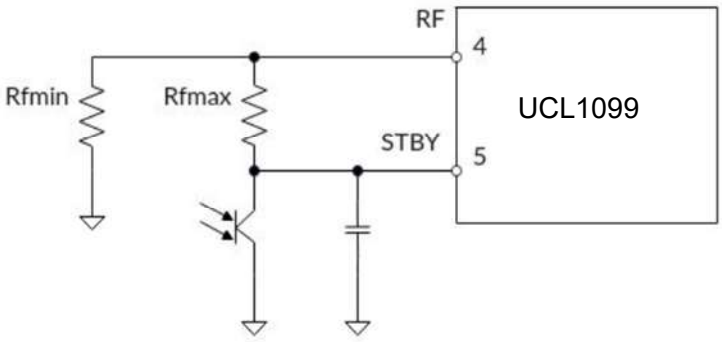


Figure 3. External Configuration for Enabling Light-Load Burst Mode Function

■ FUNCTION DESCRIPTIONS (Cont.)

RF_{max} sets the maximum operating frequency in light-load Burst mode, and the calculation formula(2) is shown below:

$$Rf_{max} = \frac{3}{8} \times \frac{RF_{min}}{f_{max} / f_{min} - 1} \quad (2)$$

The maximum switching frequency (fmax) corresponds to a load power PBurst. At this operating point, the peak current flowing through the transformer is sufficiently low to eliminate audible noise. Due to the inherent characteristics of the resonant circuit, the switching frequency is also dependent on the input voltage, which causes PBurst to vary with voltage fluctuations. To stabilize PBurst, apply the circuit illustrated in Figure 4 to feed the input line voltage signal into the feedback loop.

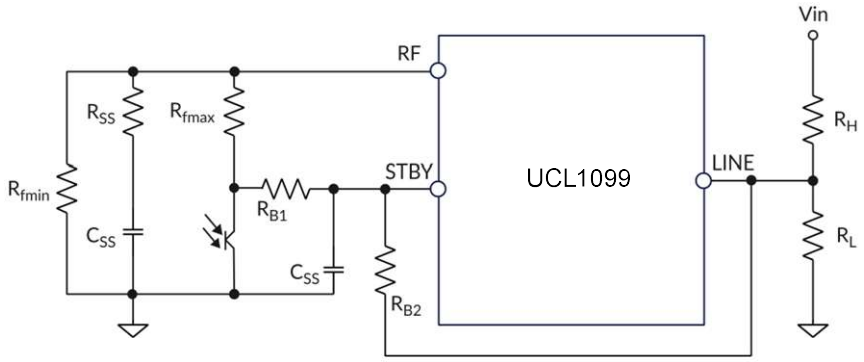


Figure 4. External Configuration for Load Burst Mode with Wide Input Voltage Range

RB1 and RB2 in Figure 4 are used to calibrate the control characteristics over a wide input voltage range (for example, 90–264 VAC). Their resistance values shall be selected based on experimental results. The total series resistance of RB1 and RB2 must be much greater than RH (20 times is recommended) to minimize the impact on the LINE pin voltage.

When the load is below PBurst, the switching frequency is clamped at the maximum value (fmax), and the output voltage exceeds the preset value. In this case, the optocoupler current increases, causing a larger voltage difference across Rfmax. As a result, the STBY pin voltage drops below V_{TH}, and the gate drive outputs are eventually disabled.

When the output voltage drops back below the preset value, the optocoupler current decreases and the STBY pin voltage rises. Once the voltage exceeds V_{TH} + 100 mV, the IC resumes outputting gate drive signals, achieving intermittent operation mode under light-load or no-load conditions.

■ FUNCTION DESCRIPTIONS (Cont.)

PFC Interface

To accommodate a wider range of application scenarios, the UTC **UCL1099** features a PFC (Power Factor Correction) interface. Under specified conditions, the PFC pin is pulled low to disable the PFC function, as shown in the figure below:

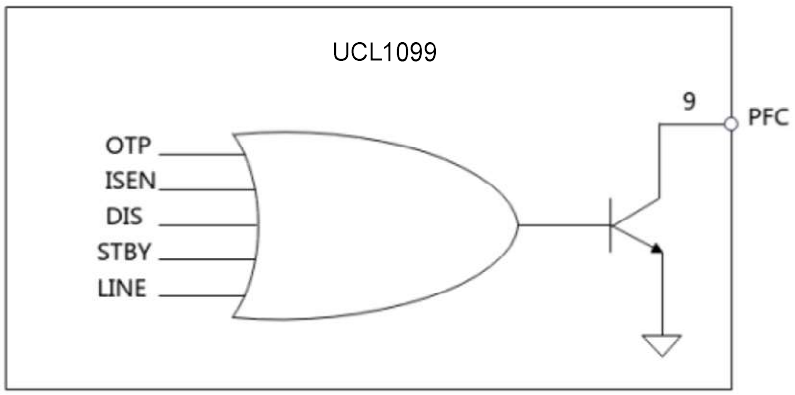


Figure 5. PFC Disable Logic Diagram

* Over-Temperature Protection (OTP)
* Second-stage Over-Current Protection (AOCP): Triggered when the DELAY pin voltage exceeds 2 V (V_{TH} 1) and does not fall back to 0.3V (V_{TH}3)
* Protection activated by a high-level signal on the DIS pin
* Light-load Burst mode operation
* LINE input voltage exceeding 6V

If the PFC interface is not used, this pin may be left floating.

Soft-Start Function

For resonant half-bridge converters, output power is inversely proportional to switching frequency. To implement soft-start, the system must start up at a relatively high switching frequency until closed-loop control takes over frequency regulation. As shown in Figure 6, when the converter is used with the The UTC **UCL1099** IC, an external series RC circuit is required to achieve soft-start.

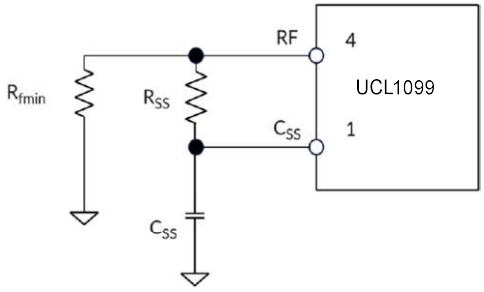


Figure 6. Soft-Start Module

■ FUNCTION DESCRIPTIONS (Cont.)

At circuit startup, the voltage at the soft-start pin (C_{SS}) is 0 V, and the soft-start resistor (R_{SS}) is connected in parallel with Rf_{min}:

$$f_{START} = \frac{1}{3 \times CT \times \left(Rf_{min} \| R_{SS}\right)} \tag{3}$$

During the startup process, the soft-start capacitor (CSS) is continuously charged until its voltage reaches the 2 V reference voltage, at this point, the current flowing through the soft-start resistor (RSS) drops to zero. This process takes approximately 5 × (RSS × CSS). During this period, the switching frequency follows an exponential curve: the frequency decays rapidly in the initial charging stage of CSS, and the decay rate gradually slows down afterwards.

After this phase, if the output voltage has not yet approached the preset value, the feedback loop takes over subsequent startup control.

With the soft-start mechanism enabled, the input current rises gradually until the output voltage stabilizes at the set point with minimal overshoot.

The selection of the soft-start RC network shall follow the formula(4) below:

$$R_{SS} = \frac{Rf_{min}}{\frac{f_{START}}{f_{min}} - 1}$$
$$C_{SS} = \frac{3 \times 10^{-3}}{R_{SS}} \tag{4}$$

Current Sensing

The block diagram of the current sensing module is shown below:

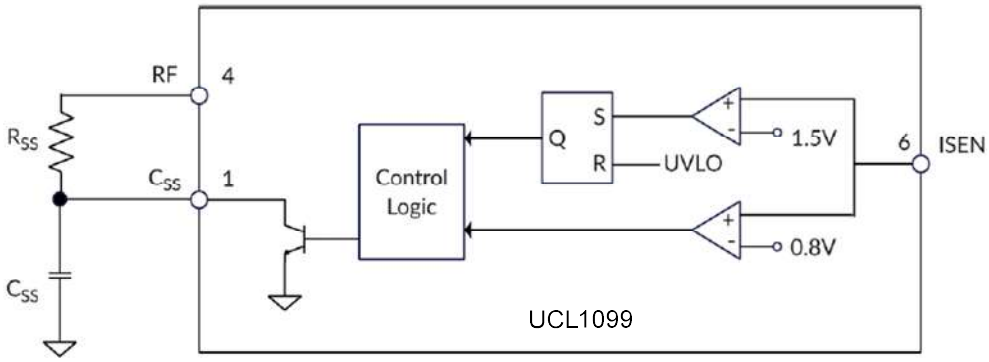


Figure 7. Block Diagram of Current Sensing Module

The IC integrates two-stage over-current protection:

The first-stage protection (OCP) is triggered when the ISEN voltage exceeds 0.8V. The comparator triggers the control logic to output a high-level signal, turning on the pull-down transistor from CSS to GND. The resulting drop in CSS voltage causes the oscillator frequency to rise sharply, thereby reducing the energy delivered to the output. When the ISEN pin voltage falls back to 0.8V, the converter resumes normal operation.

Typically, the ISEN pin voltage continues to rise under short-circuit conditions. When the ISEN pin voltage rises to 1.5V, the second-stage over-current protection (AOCP) is triggered. At this point, the IC enters a latched state and maintains extremely low power consumption.

■ FUNCTION DESCRIPTIONS (Cont.)

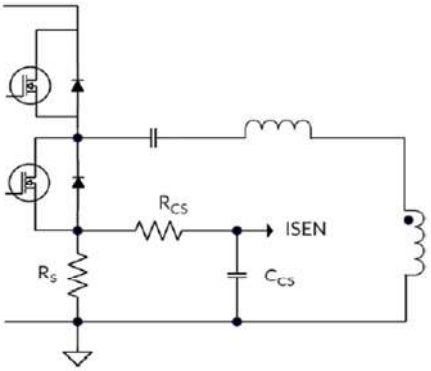


Figure 8. Over-Current Protection Schematic Diagram

There are two main types of current sensing methods: one uses a sense resistor connected in series with the low-side MOSFET; the other adopts a lossless current sensing network. The first method features simple implementation but causes additional power loss; the second method avoids resistive losses and improves system efficiency.

The calculation formula(5) for the sense resistor is given as follows:

$$RS = \frac{4}{I_{Crpk}} \quad (5)$$

The calculation of the current sensing resistor shall satisfy the following conditions:

ICrpk refers to the target peak current flowing through the primary-side MOSFET and resonant capacitor under minimum input voltage and full load conditions.

As an RC filter needs to be added between the sense resistor and the ISEN pin, its time constant shall be set to 10/fmin.

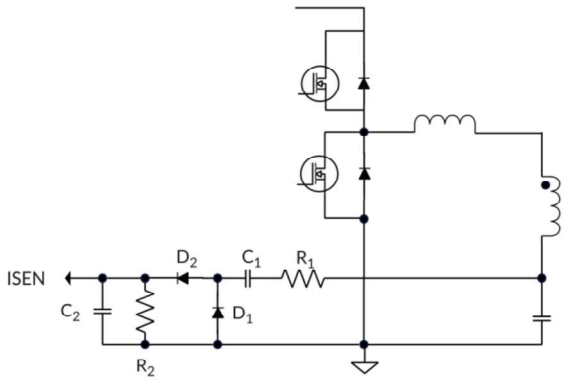


Figure 9. Current Sensing (Lossless Current Sensing Network)

Over-Current Protection (OCP) limits energy transfer from the primary side to the secondary side during overload or short-circuit conditions. However, excessive power dissipation caused by sustained high current may still damage the secondary windings and rectification devices. This controller reduces the average power dissipation during OCP via the following dual mechanisms:

Hiccup mode: After OCP is triggered, the converter enters an intermittent operation state.

Timer control: The maximum overload/short-circuit duration (t_{OC}) is set via external components CTimer and RTimer.

The first-stage protection is triggered when the ISEN voltage exceeds 0.8V, activating the internal 130μA constant current source to charge the DELAY capacitor. When the DELAY voltage reaches 2V, the switching frequency is forced down to fstart to minimize energy transfer. The 130μA current source continues charging until the DELAY voltage reaches the 3.5V turn-off threshold, at which point the output gate drive is disabled. The DELAY capacitor then discharges through the resistor to ground, and the IC restarts when the DELAY voltage falls below 0.3V.

■ FUNCTION DESCRIPTIONS (Cont.)

DIS Function

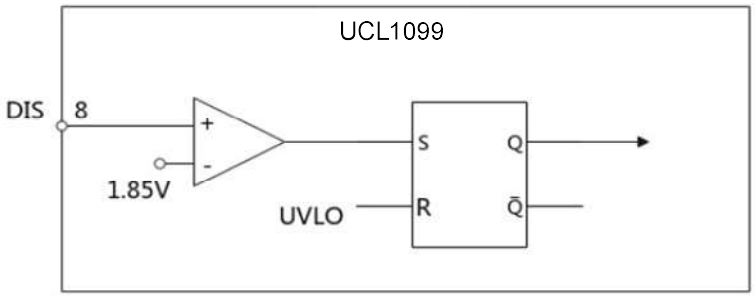


Figure 10. DIS Function Block Diagram

The DIS pin provides a simple latch function. When the DIS pin voltage exceeds 1.85V, the IC enters a latched shutdown state. Once latched, the IC exhibits significantly reduced power dissipation, and can only be reset by dropping the V_{CC} voltage below the UVLO threshold.

Input Line Voltage Sensing

The UTC **UCL1099** detects the input line voltage through the LINE pin. It ceases operation when the voltage falls below the preset threshold, and restarts automatically after the input voltage returns to normal. This function ensures that the resonant half-bridge converter always operates within the rated input voltage range. When the LINE pin voltage exceeds the internal clamp voltage, the IC triggers shutdown protection. The IC resumes normal operation only when the pin voltage drops below the clamp voltage, as illustrated below.

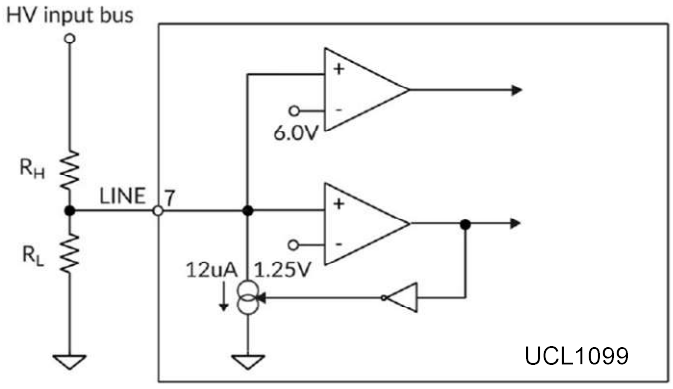


Figure 11. Input Line Voltage Sensing Block Diagram

■ FUNCTION DESCRIPTIONS (Cont.)

High-Side Gate Drive

The UTC **UCL1099** features an integrated high-side bootstrap charging diode (with an equivalent series resistance of 100 Ω) for simplified application design. An external BST capacitor supplies power to the high-side gate driver, and the integrated bootstrap diode charges this capacitor via the VCC pin. This diode simplifies the external drive circuit for the high-side switch, enabling the BST capacitor to complete charging when the low-side MOSFET is turned on, as shown below.

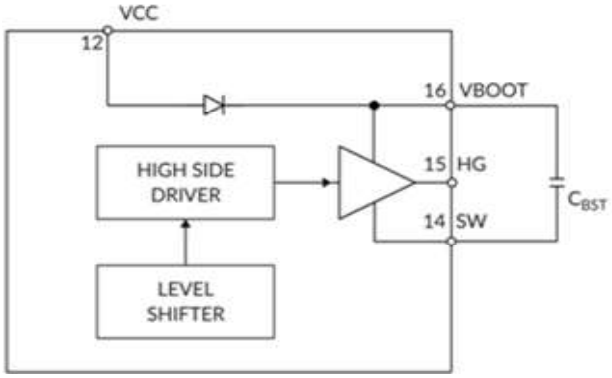


Figure 12. High-Side Gate Drive Schematic Diagram

Low-Side Gate Drive

The LG pin delivers gate drive signals to the low-side MOSFET. Per the absolute maximum ratings table, the maximum withstand voltage of the LG pin is 16 V. Long drive traces, MOSFET parasitic capacitance, and undersized gate resistance may induce oscillation, generating voltage spikes on the LG pin that exceed the withstand voltage limit. To mitigate these spikes, a 15 V Zener diode can be connected in parallel between the LG and GND pins, and placed in close proximity to the pins.

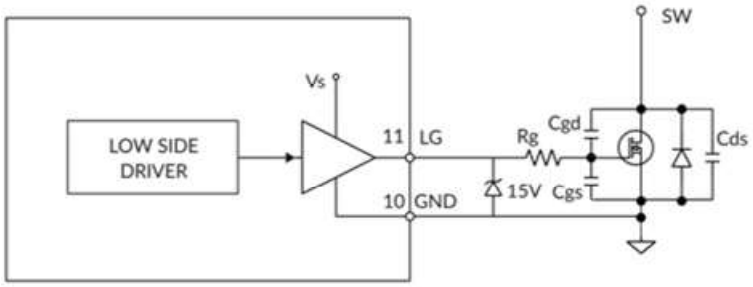
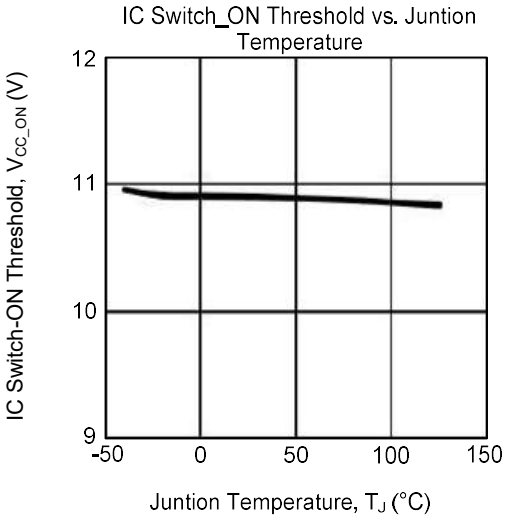
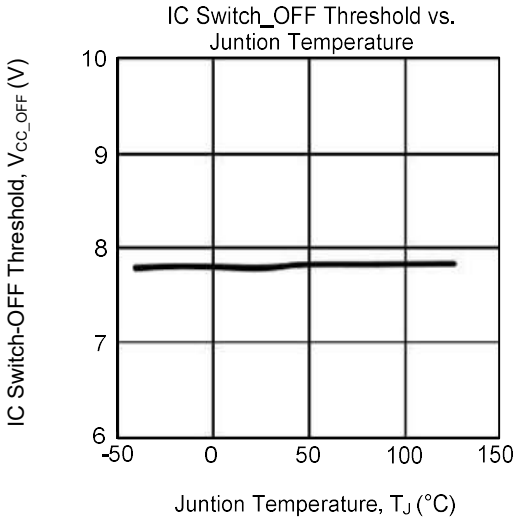
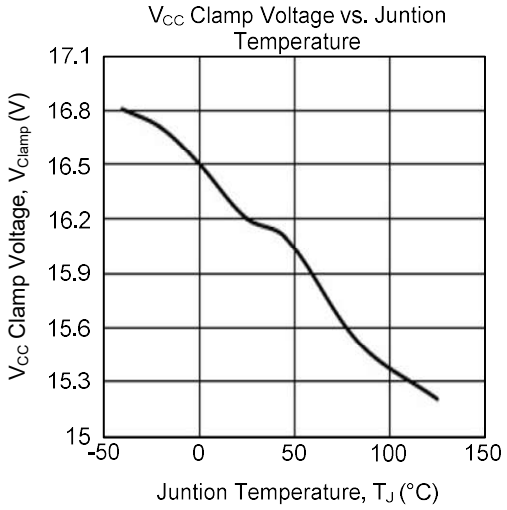


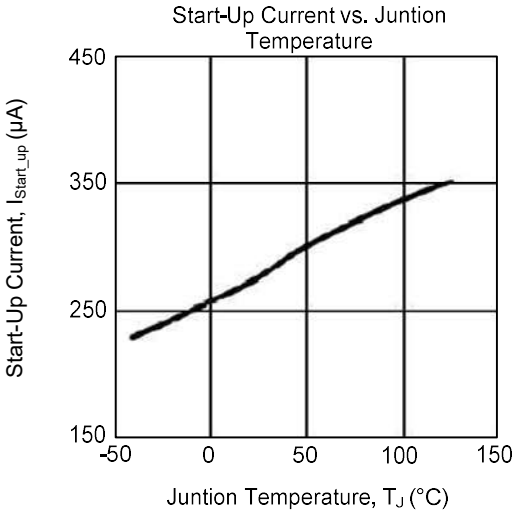
Figure 13. Low-Side Gate Drive Schematic Diagram

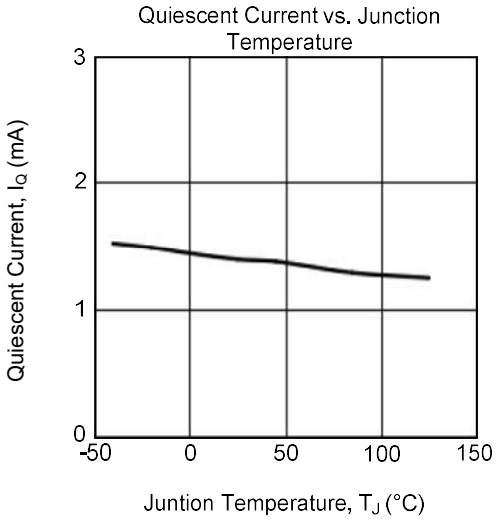
■ TYPICAL CHARACTERISTICS

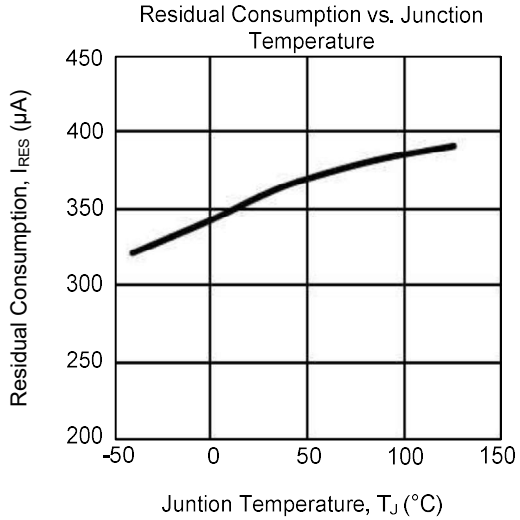






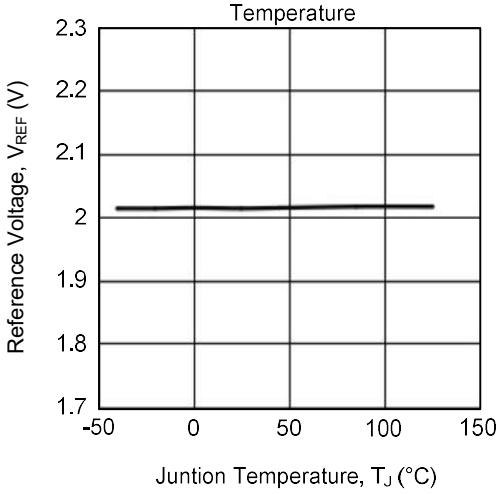




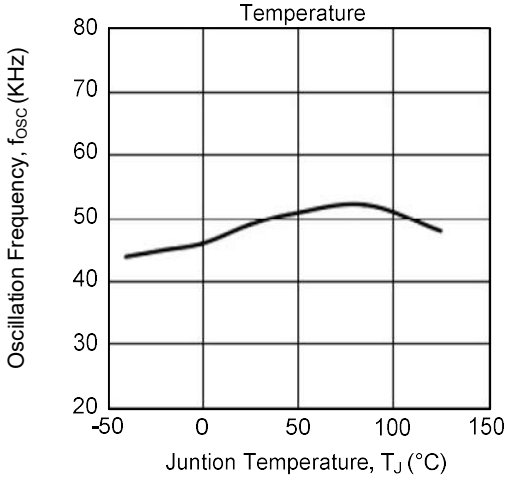


■ TYPICAL CHARACTERISTICS (Cont.)

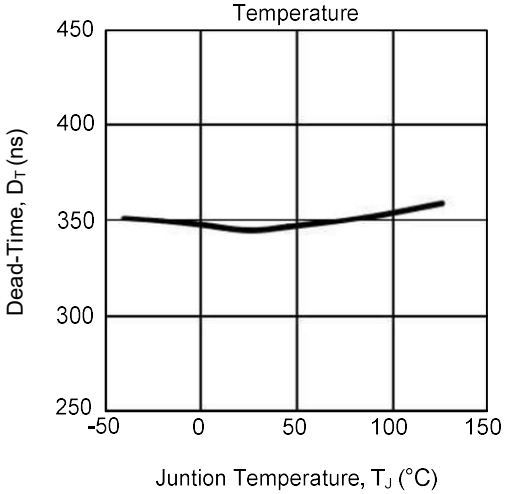
Reference Voltage vs. Junction Temperature



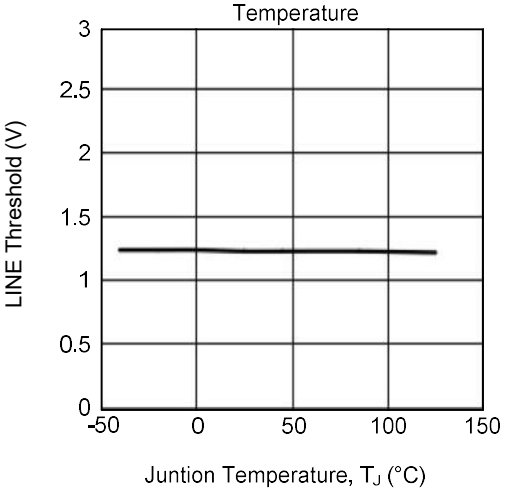
Oscillation Frequency vs. Junction Temperature



Dead-Time vs. Junction Temperature



LINE Threshold vs. Junction Temperature



LINE Current vs. Junction Temperature