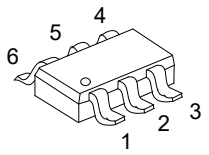
UD400601

CMOS IC

5V~40V INPUT, 600mA OUTPUT, SYNCHRONOUS STEP-DOWN CONVERTER



SOT-26

■ DESCRIPTION

The UTC **UD400601** is a synchronous buck converter with 1.2MHz switching frequency, supports an input voltage range of 5V to 40V, and can provide 600mA continuous load current.

The device achieves high-efficiency operation by integrating low RDS(ON) power tubes internally, and uses the Power Save Mode to reduce the switching frequency of the IC under light-load conditions, thereby improving light-load efficiency.

UTC **UD400601** uses the internal soft-start function to prevent possible overshoot voltage and surge current during the startup process, and achieves fast response of the loop through the Peak Current Control Mode. 1.2MHz switching frequency can prevent EMI noise problems.

The devices feature comprehensive protection features such as overcurrent limiting, input undervoltage lockout, and overtemperature shutdown.

UTC **UD400601** is packaged in SOT-26 and have a rated junction temperature range of -40°C to 125°C.

■ FEATURES

* Input Voltage Range: 5V to 40V
* 600mA Continuous Output Current
* Minimum Switching-On Time: 90ns
* 1.2MHz Switching Frequency
* Integrated 630mΩ/270mΩ Power MOSFETs
* Internal Soft-Start
* Peak Current Mode Control
* Power Save Mode and PWM Mode
* Short Circuit Protection
* Thermal Shutdown
* Green & Pb Free

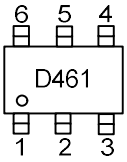
■ ORDERING INFORMATION

Ordering Number	Package	Packing
UD400601G-AG6-R	SOT-26	Tape Reel

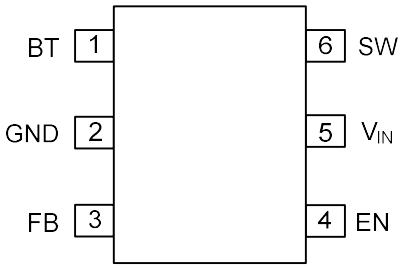
UD400601G-AG6-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) AG6: SOT-26
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



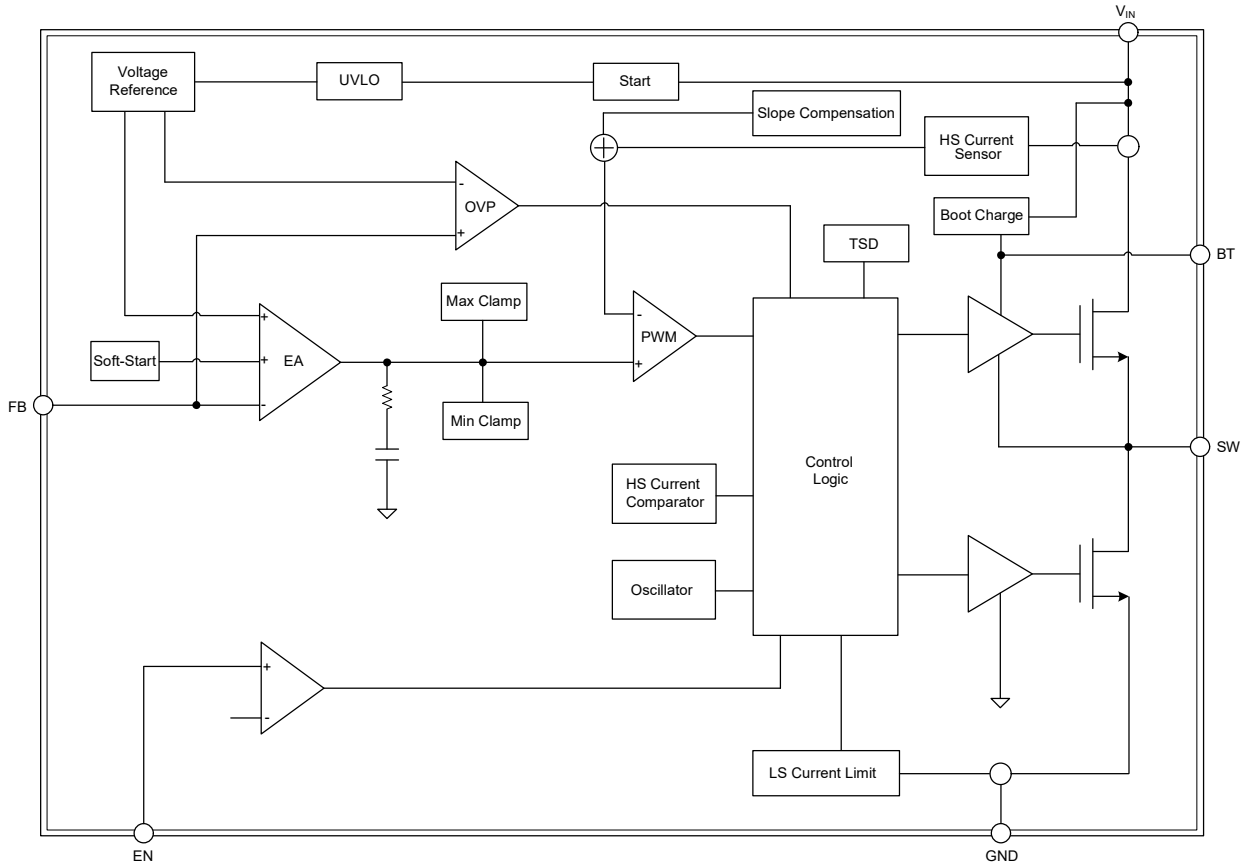
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	BT	Place a capacitor between the BT and SW pins to provide the required gate drive voltage for the high-side power MOS.
2	GND	Ground Pin.
3	FB	Feedback Input. Different output voltages can be obtained by matching different external voltage dividing resistors.
4	EN	Enable logic input. Do not float.
5	V_{IN}	Input power pin.
6	SW	Switching Pin. SW is the switching node that supplies power to the output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_J = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	V_I	-0.3 ~ 42	V
	EN		-0.3 ~ V_{IN}+0.3	V
	BT-SW		-0.3 ~ 5.5	V
	FB		-0.3 ~ 5.5	V
	SW		-0.3 ~ V_{IN}+0.3	V
	SW (10ns Transient)		-4.5 ~ 42	V
Operating Junction Temperature		T_J	-40 ~ 150	°C
Storage Temperature Range		T_{STG}	-65 ~ 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (T_J = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	V_I	5 ~ 40	V
	EN		-0.1 ~ V_{IN}	V
	FB		-0.1 ~ 4.5	V
Operating Junction Temperature		T_J	-40 ~ 125	°C

■ ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{IN} = 12V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
Non Switching Supply Current	I_Q	EN = 2V, V_{FB} = 0.9V		46	66	μA
Shutdown Supply Current	I_{SD}	EN=0		2	5	μA
LOGIC THRESHOLD						
EN Terminal Input Threshold	V_{IH}	Rising		1.23	1.40	V
	V_{IL}	Falling	0.95	1.1		V
EN Hysteresis	V_{EN_HYS}			130		mV
EN Terminal Leakage Current	I_{EN}	V_{EN}=12V		0.1	0.5	μA
V_{FB} VOLTAGE						
V_{FB} Threshold Voltage	V_{FB}		784	800	816	mV
POWER STAGE						
High-Side FET On-Resistance	R_{DSON_HS}	Ta=25°C, V_{BT}-V_{SW}=5.5V		630		mΩ
Low-Side FET On-Resistance	R_{DSON_LS}	Ta=25°C		270		mΩ
CURRENT LIMIT						
	I_{LIM_HS}	Ta=25°C	0.9	1.2	1.6	A
OVER TEMPERATURE PROTECTION						
Thermal Shut Down Threshold (Note 1)	T_{SHDN}	Shutdown Temperature		150		°C
		Hysteresis		20		°C
OSCILLATOR						
Switching Frequency	F_{SW}			1.2		MHz
UVLO						
UVLO Threshold	V_{UVLO}	Wake up V_{IN} Voltage		4.65	4.95	V
		Shutdown V_{IN} Voltage		4.33		V
		Hysteresis V_{IN} Voltage		320		mV

Note: Specified by design.

■ DETAILED DESCRIPTION

Overview

UTC **UD400601** is an efficient and reliable synchronous buck chip that can provide up to 600mA continuous load current. The device's working mode has been optimized to enter PSM (Power Save Mode) mode under light load conditions, adaptively adjust the switching frequency, reduce switching losses, thereby improving efficiency at this time.

Peak Current Mode Control

UTC **UD400601** uses peak current control mode to achieve fast loop response. The voltage change of the switch node (SW) of the device is realized through the complementary control of the MOS on the high and low sides of the device. When the high-side MOS is turned on, the inductor current rises linearly, and the slope depends on the input and output voltage and the inductor value. When the low-side MOS is turned on, the inductor current decreases linearly, and its slope depends on the output voltage and the inductor value. In order to ensure reliable operation of the device and prevent breakdown, after the high-side MOS is turned off, there is always a very short dead time before the low-side MOS can be turned on.

The device achieves precise output voltage regulation through an external voltage feedback loop, and the output voltage also serves as a reference command for the peak current control loop to control the inductor peak current. In the CCM stage, the device adopts a fixed-frequency peak control mode. In the DCM stage, due to the reduced switching frequency, it is a variable frequency peak current control mode. Specifically, the reference base of the current is determined by the voltage feedback loop. When the high-side MOS detects that the peak current of the inductor exceeds the current reference, the high-side MOS immediately turns off, and then the low-side power tube turns on, thereby controlling the inductor current.

Power Save Mode

UTC **UD400601** improves efficiency under light load conditions through built-in PSM mode. When the load current decreases, the average current of the inductor also decreases. When the valley value of the inductor current is detected to be zero, the controller turns off the low-side MOS. When the load current decreases further, the DCM stage will be entered. Since the switch on-time in PSM mode is the same as the CCM phase, this means that the output capacitor absorbs the same amount of charge during the high-side MOS on-time each time. Therefore, under light load, it takes longer to discharge the voltage at the output capacitor below the reference voltage. During this period, the MOS on both high and low sides will not be turned on, thereby reducing switching losses and improving the working efficiency of the device. But the output ripple at this time will increase slightly.

Over-Current Protection

The high-side and low-side MOS inside the device have current limiting functions. This function is activated in the initial power-on, output overload and output short circuit conditions, which can effectively prevent the inductor current from running out of control.

Minimum ON/OFF-Time and Frequency Fold-Back

The minimum on and off times of the UTC **UD400601** high-side MOS are 90ns (T_{ON_MIN}) and 100ns (T_{OFF_MIN}) respectively. T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range.

If the parasitic effects of components are ignored, the maximum duty cycle, minimum duty cycle of the device under ideal conditions, and the maximum V_{IN} and minimum V_{IN} supported by the device at a given output voltage are calculated as follows:

$$D_{MIN}=T_{ON\_MIN}\times f_{SW} \quad (1)$$

$$D_{MAX}=T_{OFF\_MIN}\times f_{SW} \quad (2)$$

$$V_{IN\_MAX}=\frac{V_{OUT}}{D_{MIN}} \quad (3)$$

$$V_{IN\_MIN}=\frac{V_{OUT}}{D_{MAX}} \quad (4)$$

■ DETAILED DESCRIPTION (Cont.)

Soft-Start

In order to prevent overshoot voltage and surge current phenomena that may occur during device startup, the device achieves a monotonic climb of the output voltage through a built-in soft-start function.

Thermal Shutdown

In order to avoid equipment damage due to over-temperature, when the IC junction temperature exceeds the maximum threshold (typical 150°C), thermal shutdown will be triggered immediately and the device will stop working. Since the hysteresis value of temperature protection is approximately 20°C, that is, when the junction temperature is lower than 130°C, the device will automatically resume work through soft start.

■ APPLICATION INFORMATION

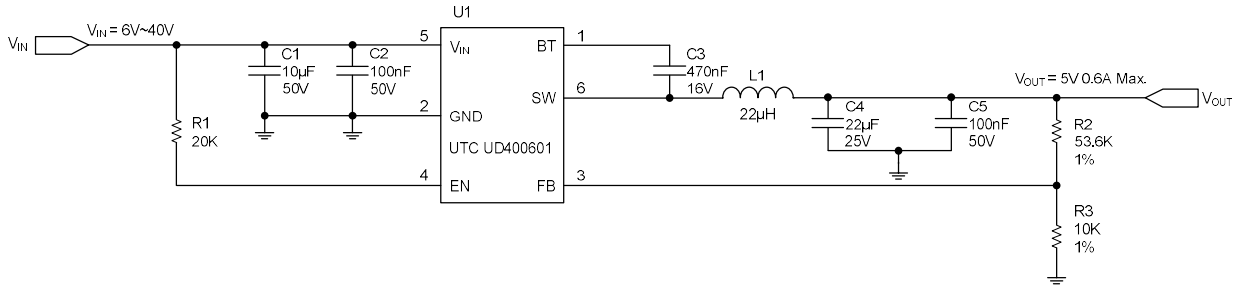


Figure 1. UTC UD400601 Reference Design for 5V, 0.6A Application

Design Requirements

1. If needed, 1% resistors R2 and R3 can be selected to improve the accuracy of the output voltage.
2. Increasing the resistance of R2 and R3 can improve the efficiency of the device under light load conditions. It should be noted that too high a resistance value will increase its sensitivity to noise.
3. This device requires a decoupling capacitor. It is recommended to use a capacitor greater than 10uF as a decoupling capacitor, and add a 0.1uF capacitor to provide additional high-frequency waves.
4. A 0.47μF ceramic capacitor must be connected between the BT and SW pins for proper operation.

Table 1. Recommended Component Values

V_{OUT}(V)	C_{IN}(μF)	L1(μH)	C_{OUT}(μF)	R2(kΩ)	R3(kΩ)
0.8	33	3.3	47	0	1000
3.3	10	10	10	31.6	10
5	10	22	22	53.6	10
12	10	47	47	147	10.5
24	10	33	22	464	16

Set Output Voltage

As shown in the figure 1, the output voltage value of UTC **UD400601** can be set by adjusting the resistance values of R2 and R3. The specific calculation formula is as follows, where V_{FB} equals 0.8V:

$$R_2 = \frac{(V_{OUT} - V_{FB}) \times R_3}{V_{FB}} \quad (5)$$

■ DETAILED DESCRIPTION (Cont.)

Output Inductor Selection

The minimum inductor value required in the application is mainly determined by the ripple coefficient of the inductor current (K_{IND}), where K_{IND} is defined as the ratio of the inductor ripple current (I_{RIPPLE}) to the load current (I_{OUT}). The value of K_{IND} can be understood as the result of a trade-off between system efficiency and peripheral device cost. K_{IND} will also affect the selection of the output capacitor. Generally speaking, the following criteria can be used for the value of K_{IND}.

For output capacitors with low ESR, K_{IND} is generally 0.4. For output capacitors with higher ESR, a K of 0.2 will usually give better results.

On the premise of determining K_{IND}, the minimum inductance value of the inductor (L_{MIN}) can be determined by Equation 6. In addition, the selection of the inductor must also consider whether its RMS current (I_{L_RMS}) and peak current (I_{PEAK}) meet the requirements. The specific calculation formulas are given by Equation 7, 8 and 9.

$$L_{MIN}=\frac{V_{OUT}}{V_{IN\_MAX}\times f_{FW}}\times\frac{(V_{IN\_MAX}-V_{OUT})}{I_{OUT}\times K_{IND}} \quad (6)$$

$$I_{RIPPLE}=\frac{(V_{IN\_MAX}-V_{OUT})\times V_{OUT}}{V_{IN\_MAX}\times L\times f_{SW}} \quad (7)$$

$$I_{L\_RMS}=\sqrt{\frac{1}{12}\times\left(\frac{(V_{IN\_MAX}-V_{OUT})\times V_{OUT}}{V_{IN\_MAX}\times L\times f_{SW}}\right)^2+(I_{OUT})^2} \quad (8)$$

$$I_{PEAK}=I_{OUT}+\frac{I_{RIPPLE}}{2} \quad (9)$$

Output Capacitor

The selection of the output capacitor usually needs to consider three factors. The capacitor will affect the loop stability of the system, the output voltage ripple V_{O_RIPPLE} under steady-state operating conditions, and the output voltage ripple ΔV_{OUT} under load transient changes. The determination of the final capacitance value of the capacitor needs to meet these three conditions at the same time.

The minimum output capacitance value required under steady-state operation can be calculated by Equation 10, where V_{O_RIPPLE} is usually required to be no greater than 0.5% of the target output voltage V_{OUT}.

$$C_{OUT}>\frac{I_{RIPPLE}}{8\times f_{SW}\times V_{O\_RIPPLE}} \quad (10)$$

When the load changes from a heavy-load I_{OH} to a light-load I_{OL}, the output capacitor needs to absorb the excess energy in the process to maintain the output voltage from overshooting. The minimum output capacitance value required under this condition can be calculated by Equation 11:

$$C_{OUT}>L\times\frac{(I_{OH})^2-(I_{OL})^2}{(V_{OUT}+\Delta V_{OUT})^2-(V_{OUT})^2} \quad (11)$$

When the load changes from light load to heavy load, since the converter requires a certain response time to adjust, the output capacitor needs to maintain the output voltage within this time without dropping. Under normal circumstances, the response time is required to be 2 working cycles, the drop value of the output voltage is not greater than 4% of the target voltage, the light load is 25% of the full load current, and the heavy load is 75% of the full load current. The minimum output capacitance value required under this condition can be calculated by Equation 12:

$$C_{OUT}>\frac{2\times(I_{OH}-I_{OL})}{f_{SW}\times\Delta V_{OUT}} \quad (12)$$

■ DETAILED DESCRIPTION (Cont.)

Taking into account the influence of the output capacitor ESR, the maximum value of ESR can be calculated through Equation 13:

$$R_{ESR} < \frac{V_{O\_RIPPLE}}{I_{RIPPLE}} \quad (13)$$

In order to operate reliably, the maximum ripple current rms value allowed to flow through the output capacitor must also meet the design requirements. This value can be obtained by Equation 14:

$$I_{COUT(RMS)} = \frac{V_{OUT} \times (V_{IN\_MAX}) \times V_{OUT}}{\sqrt{12} \times V_{IN(MAX)} \times L \times f_{SW}} \quad (14)$$

Input Capacitor

The capacitance of the input capacitor determines the size of the input voltage ripple V_{I_RIPPLE}. V_{I_RIPPLE} can be calculated by Equation 15. Since V_{I_RIPPLE} takes the maximum value when the duty cycle is 0.5, under the given requirement of expected V_{I_RIPPLE}, the minimum capacitance of the required input capacitor can be obtained through Equation 16. The root mean square value of the ripple current allowed to flow through the capacitor can be calculated using Equation 17.

$$V_{I\_RIPPLE} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}} \quad (15)$$

$$V_{I\_RIPPLE} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} \quad (16)$$

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{(V_{IN\_MIN} - V_{OUT})}{V_{IN\_MIN}}} \quad (17)$$

■ TYPICAL APPLICATION CIRCUIT

Schematic