



UT4315

POWER MOSFET

P-CHANNEL ENHANCEMENT MODE

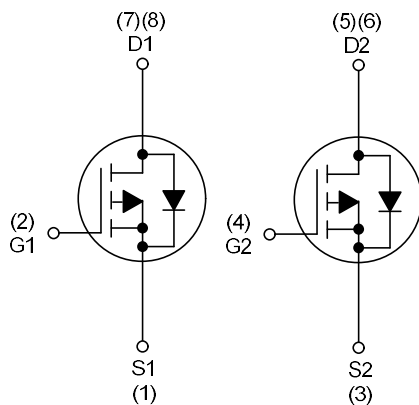
DESCRIPTION

The UTC **UT4315** uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

- * $R_{DS(ON)} \leq 15 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -18\text{A}$
 $R_{DS(ON)} \leq 22 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -12\text{A}$
- * Low capacitance
- * Optimized gate charge
- * Fast switching capability
- * Avalanche energy specified
- * Green Product

SYMBOL

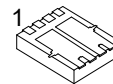


ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UT4315G-P5060-R	PDFN5×6	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

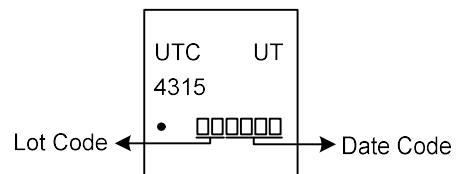
Note: Pin Assignment: G: Gate D: Drain S: Source

UT4315G-P5060-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P5060: PDFN5×6 (3) G: Halogen Free and Lead Free
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PDFN5×6

■ MARKING



■ **ABSOLUTE MAXIMUM RATING** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	-52	A
	Pulsed (Note 2)	I_{DM}	-80	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	30	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.2	V/nS
Power Dissipation		P_D	34	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = -30\text{A}$, $V_{DD} = -25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq -30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	75	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.68	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

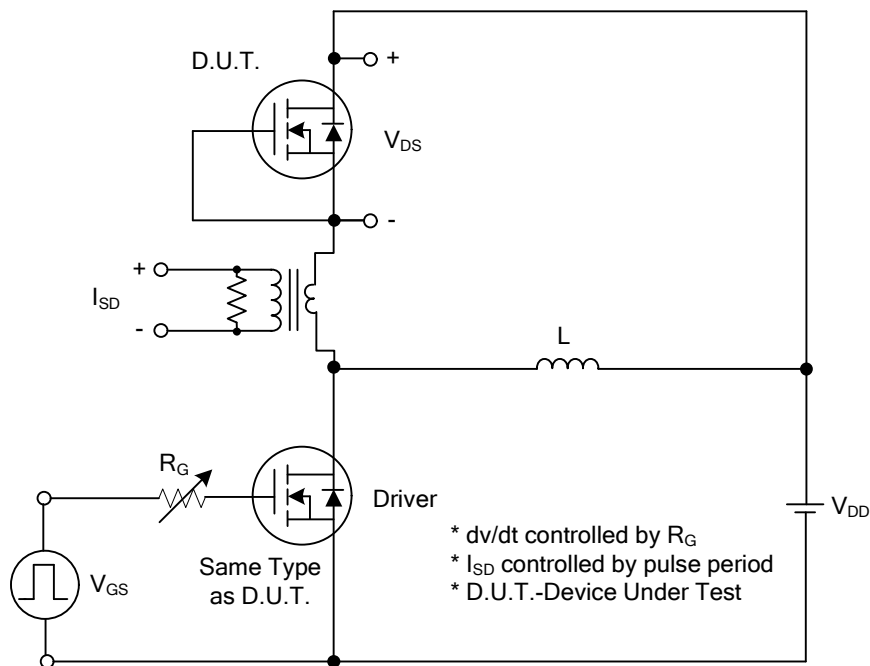
■ **ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	-40			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V			-1	μA
Gate- Source Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =+20V			+100	nA
		V _{DS} =0V, V _{GS} =-20V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note 1)	R _{DS(ON)}	V _{GS} =-10V, I _D =-18A			15	mΩ
		V _{GS} =-4.5V, I _D =-12A			22	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =-20V, f=1.0MHz		3018		pF
Output Capacitance	C _{OSS}			333		pF
Reverse Transfer Capacitance	C _{RSS}			266		pF
SWITCHING PARAMETERS (Note 2)						
Total Gate Charge (Note 1)	Q _G	V _{DS} =-32V, V _{GS} =-10V, I _D =-52A (Note 1, 2)		51		nC
Gate to Source Charge	Q _{GS}			7		nC
Gate to Drain Charge	Q _{GD}			12		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DS} =-20V, V _{GS} =-10V, I _D =-52A, R _{GS} =3.3Ω (Note 1, 2)		9		ns
Rise Time	t _R			18		ns
Turn-OFF Delay Time	t _{D(OFF)}			89		ns
Fall-Time	t _F			52		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				-52	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				-80	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _F =-52A, V _{GS} =0V			-1.2	V
Reverse Recovery Time (Note 1)	t _{rr}	I _F =-30A, V _{GS} =0V		80		ns
Reverse Recovery Charge	Q _{rr}	dI _F /dt=100A/μs		143		nC

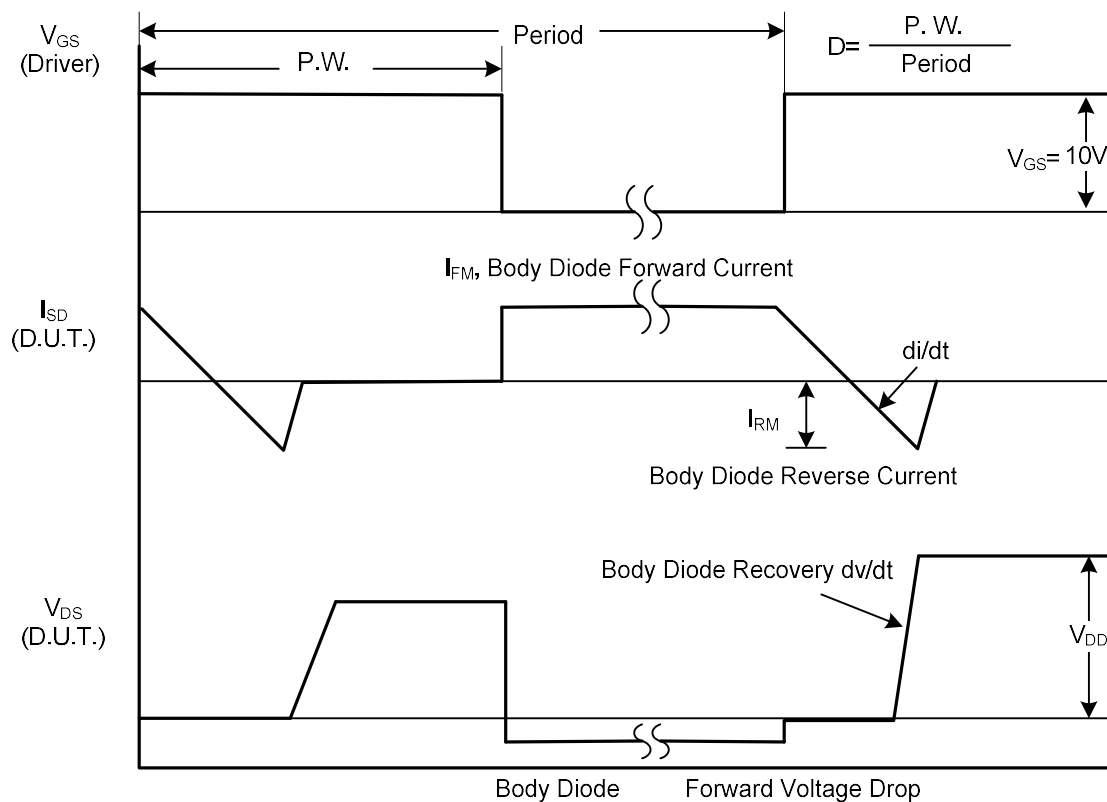
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

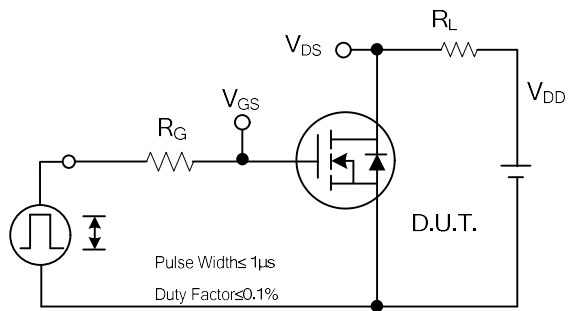


Peak Diode Recovery dv/dt Test Circuit

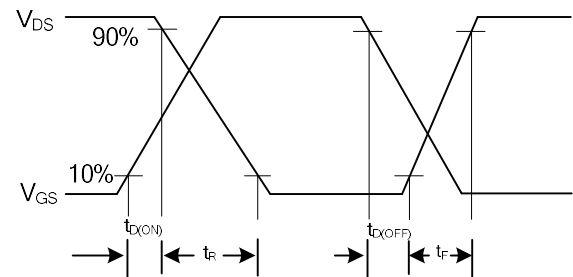


Peak Diode Recovery dv/dt Waveforms

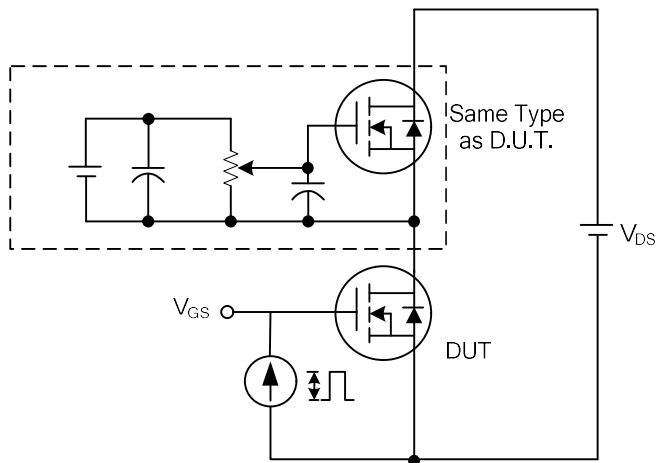
■ TEST CIRCUITS AND WAVEFORMS



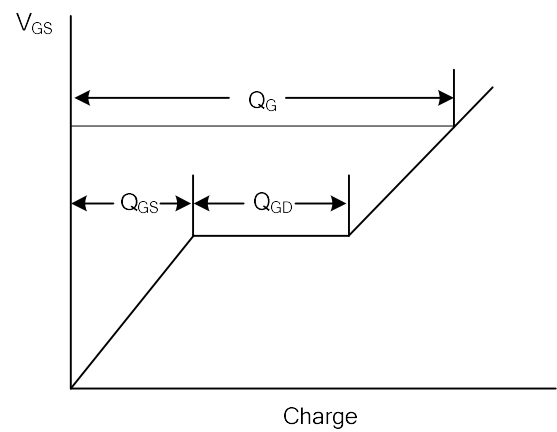
Switching Test Circuit



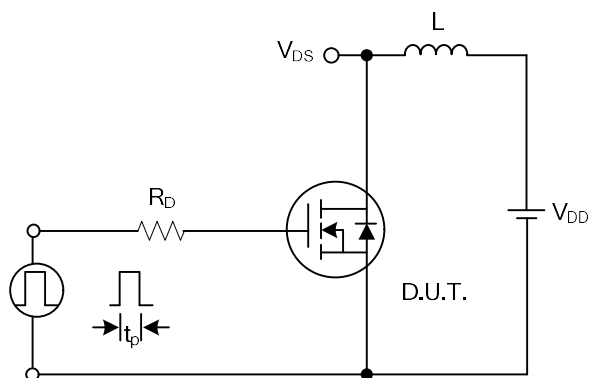
Switching Waveforms



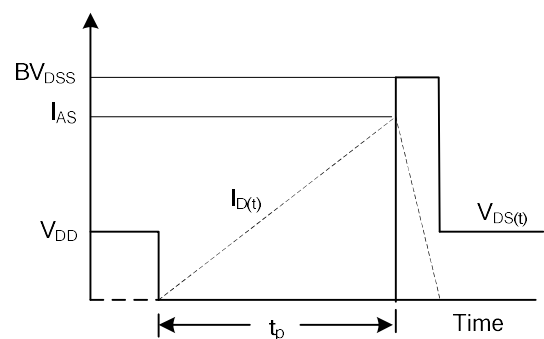
Gate Charge Test Circuit



Gate Charge Waveform

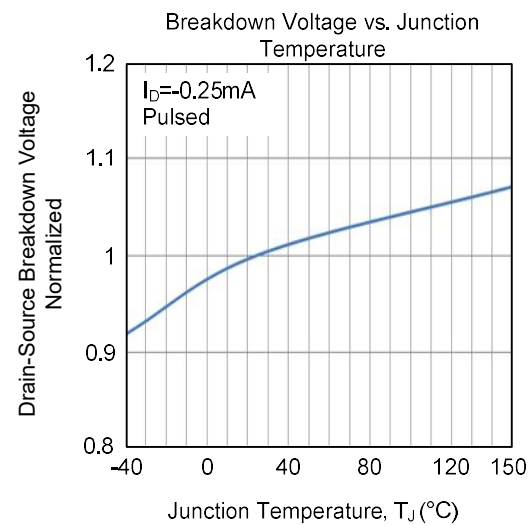
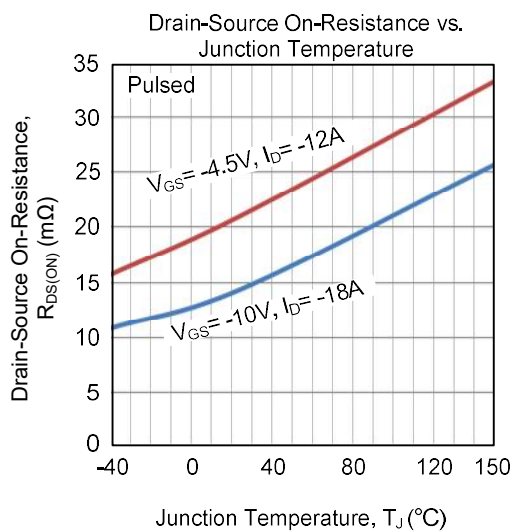
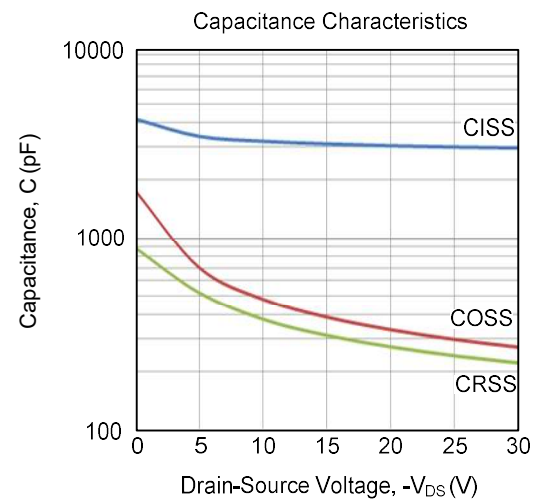
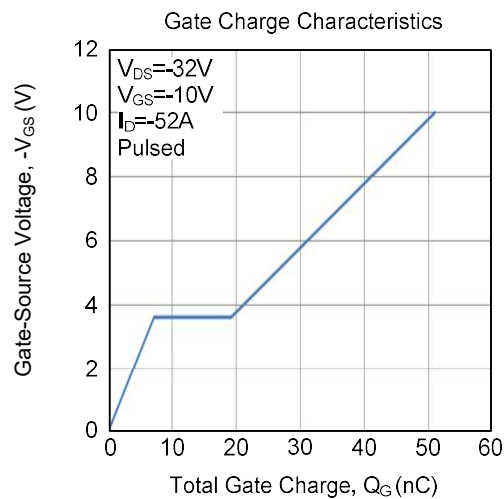
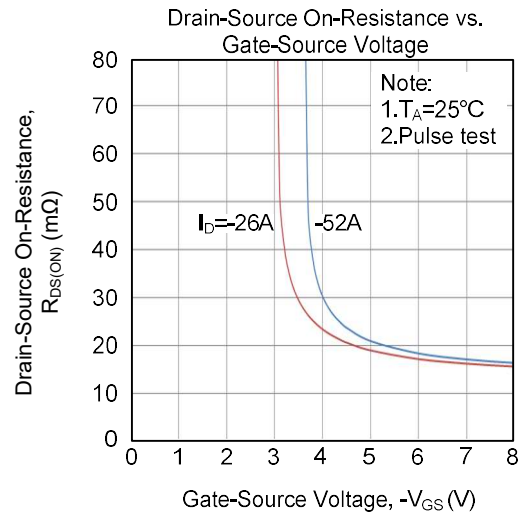
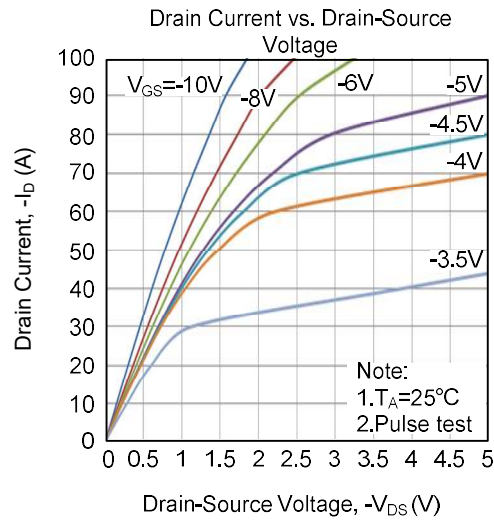


Unclamped Inductive Switching Test Circuit

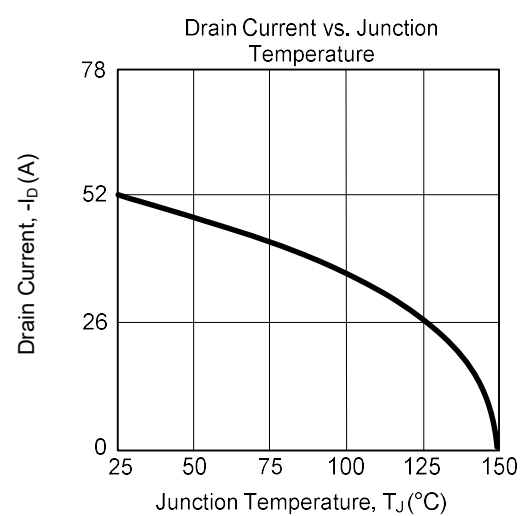
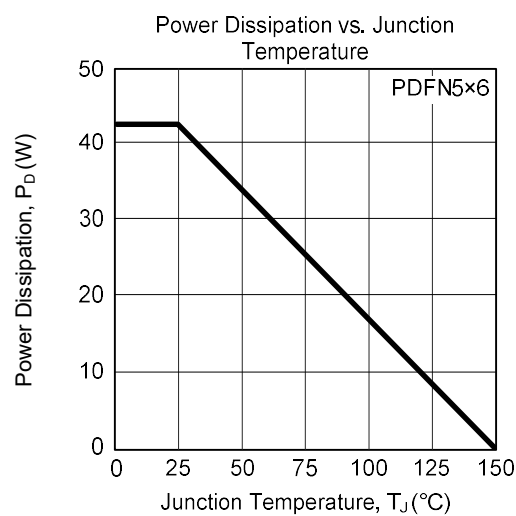
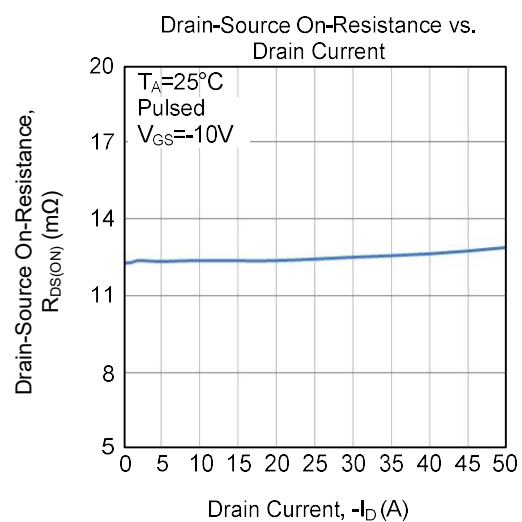
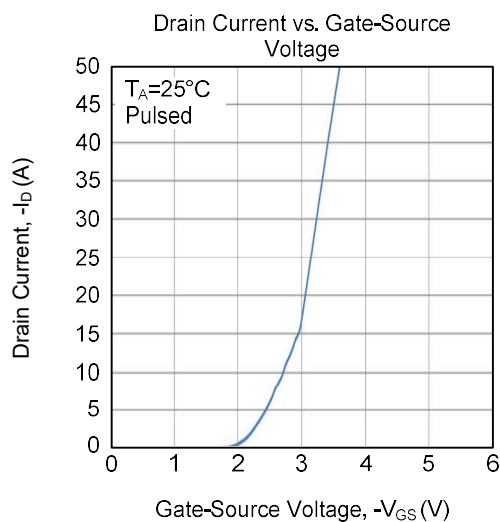
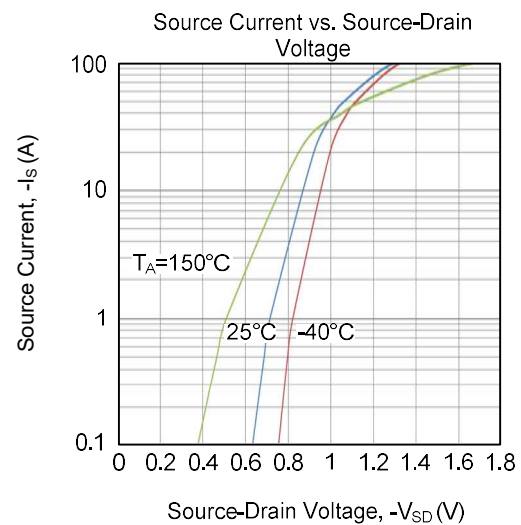
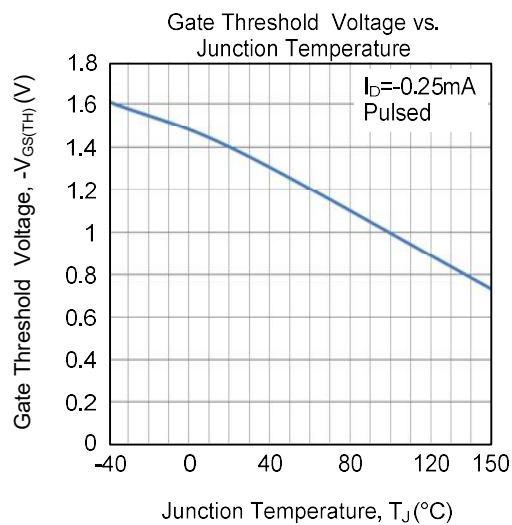


Unclamped Inductive Switching Waveforms

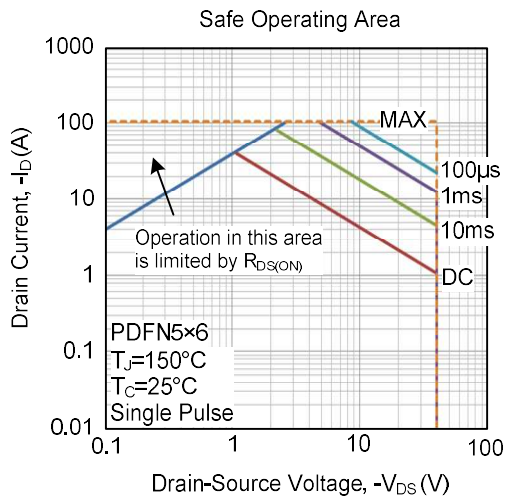
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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