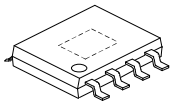
4.5V~60V INPUT, 5A OUTPUT, NON-SYNCHRONOUS BUCK CONVERTER



HSOP-8

■ DESCRIPTION

The UTC **UD60501** is an asynchronous buck converter that supports an input voltage range of 4.5V to 60V and delivers 5A continuous load current. The device has an operating frequency of 100KHz to 2.5MHz and supports setting the switching frequency through an external clock.

The device achieves high-efficiency operation by integrating a low RDS(ON) MOS internally, and uses the PSM (power-saving mode) to reduce the switching frequency of the IC under light-load conditions, thereby improving light-load efficiency.

The device's undervoltage lockout is internally set to 4.3V and supports customization of the undervoltage lockout threshold through EN pin.

UTC **UD60501** utilizes the internal soft-start function to prevent possible overshoot voltage and surge current during startup, achieves fast response of the loop through current control mode, and supports flexible and simple selection of external compensation components.

The device features comprehensive protection features such as overcurrent limit, frequency foldback, input undervoltage lockout, overvoltage protection, and thermal shutdown.

The UTC **UD60501** is available in an eSOP8L package and has a rated junction temperature range of -40°C to 150°C.

■ FEATURES

* Input Voltage Range: 4.5V to 60V
* 5A Continuous Output Current
* Integrated 95mΩ Power MOSFET
* 100KHZ to 2.5MHz Fixed Switching Frequency
* Synchronizes to External Clock
* Low Dropout at Light Loads
* Power Save Mode and PWM Mode
* Current Mode Control
* Internal Soft-Start
* Adjustable UVLO Voltage
* Short Circuit Protection
* Thermal Shutdown
* Green & Pb Free

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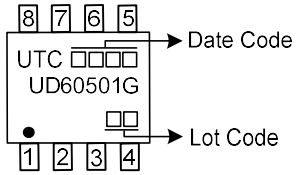
■ ORDERING INFORMATION

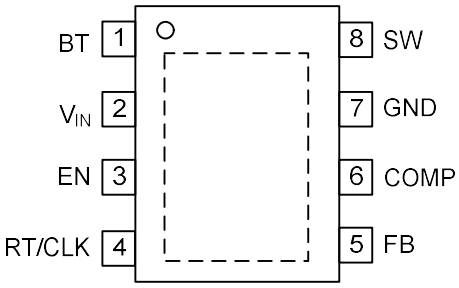
Ordering Number	Package	Packing
UD60501G-SH2-R	HSOP-8	Tape Reel

UD60501G-SH2-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) SH2: HSOP-8 (3) G: Halogen Free and Lead Free

■ MARKING



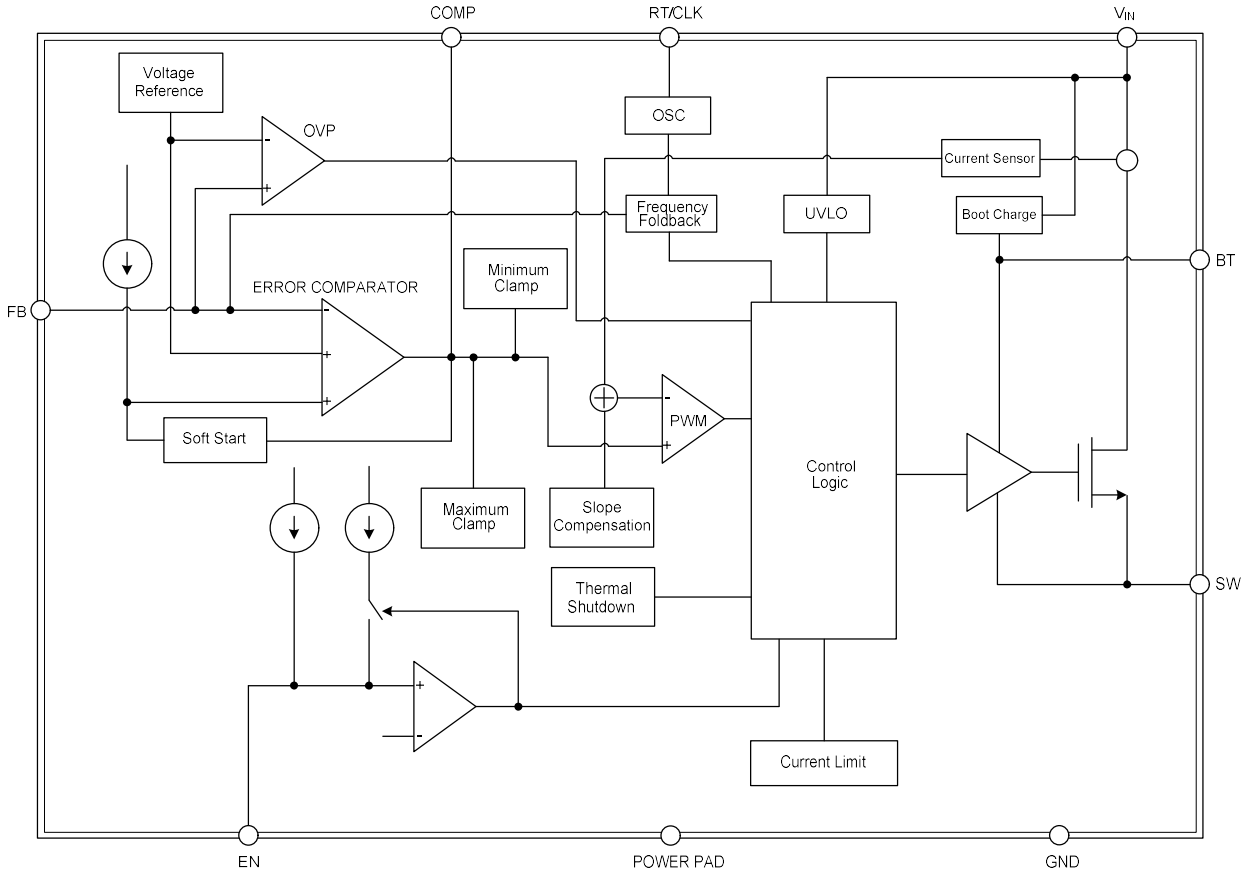
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	BT	Place a capacitor between the BT and SW pins to provide the required gate drive voltage for the high-side power MOS.
2	V_{IN}	Input power pin.
3	EN	Enable logic input.
4	RT/CLK	Frequency setting and external clock signal input pin. Connect a resistor from this pin to ground to set the frequency or connect to a clock signal to synchronize the frequency.
5	FB	Feedback Input. Different output voltages can be obtained by matching different external voltage dividing resistors.
6	COMP	Error amplifier output pin. To achieve frequency compensation.
7	GND	Ground pin.
8	SW	Switching Pin. SW is the switching node that supplies power to the output.
Exposed Pad	GND	The exposed pad must be connected the GND pin.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_J=25°C, unless otherwise specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	V_I	-0.3 ~ 65	V
	EN		-0.3 ~ 6	V
	BT		72	V
	FB		-0.3 ~ 6	V
	COMP		-0.3 ~ 6	V
	RT/CLK		-0.3 ~ 6	V
Output Voltage Range	BT-SW	V_O	6.5	V
	SW		-0.6 ~ 65	V
	SW (10ns Transient)		-2 ~ 65	V
Junction Temperature		T_J	-40 ~ +150	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (T_J=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	4.5 ~ 60	V
Output Voltage Range	V_{OUT}	0.8 ~ 57	V
Operating Junction Temperature	T_J	-40 ~ +150	°C

■ ELECTRICAL CHARACTERISTICS (T_J = -40 ~ 150°C, V_{IN} =4.5 ~ 60V, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
Non-Switching Supply Current	I_Q	V_{FB} = 0.9V, 25°C		160	240	μA
Shutdown Supply Current	I_{SD}	EN = 0.5V, 25°C, 4.5V ≤ V_{IN} ≤ 60V		2.7	5.0	μA
LOGIC THRESHOLD						
EN Terminal Input Threshold	V_{ENTH}	Rising and Falling		1.2		V
EN Input Current	I_{EN}	Enable Threshold + 50mV		-4.9		μA
		Enable Threshold - 50mV	-1.6	-1.2	-0.9	μA
Hysteresis Current	I_{HYS}		-4.4	-3.7	-3.0	μA
V_{FB} VOLTAGE						
Voltage Reference	V_{FB}		0.788	0.8	0.812	V
POWER STAGE						
On-Resistance	R_{DSON_HS}	V_{BT} - V_{SW} = 5.5V, V_{IN}=12V		95	165	mΩ
CURRENT LIMIT						
Current Limit	I_{OCL}	Open Loop	6.0	7.5		A
Current Limit Threshold Delay	I_{OCL_HYS}			65		ns
OVER TEMPERATURE PROTECTION						
Thermal Shut Down Threshold	T_{SHDN}	Shutdown Temperature		165		°C
Thermal Shut Down Threshold Hysteresis	T_{SHDN_HYS}			10		°C
OSCILLATOR						
Frequency Range	f_{SW}	R_T = 200kΩ	400	500	600	kHz
Frequency Range Using RT Mode			100		2500	kHz
Frequency Range Using CLK Mode			150		2400	kHz
RT/CLK High Threshold				1.5	2.0	V
RT/CLK Low Threshold			0.5	1.2		V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
UVLO Threshold	V_{UVLO}	Rising		4.3	4.45	V
		Falling	3.85	4.0		V
UVLO Hysteresis	V_{UVLO_HYS}			0.3		V
ERROR AMPLIFIER						
FB Input Current				0		nA
Error Amplifier Transconductance (gm)	GM	$-2\mu A < I_{COMP} < 2\mu A$, V_{COMP} = 1V		360		μA/V
Error Amplifier DC Gain		V_{FB} = 0.8V		20000		V/V
Error Amplifier Unity Gain Bandwidth		COMP Terminal 15pF to GND		3.2		MHz
Error Amplifier Source Current		V_{COMP} = 1V, V_{FB} = 0.7V		-32		μA
Error Amplifier Sink Current		V_{COMP} = 1V, V_{FB} = 0.9V		32		μA
COMP to Switch Current Transconductance				14		A/V

■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START						
Soft-Start Time	T_{SS}	f_{SW} = 100kHz, 10% to 90%		10		ms
		f_{SW} = 600kHz, 10% to 90%		1.5		ms
		f_{SW} = 2MHz, 10% to 90%		0.3		ms
TIMING RESISTOR AND EXTERNAL CLOCK						
Minimum CLK Pulse Width				30		ns
RT/CLK falling edge to SW Rising Edge Delay		External Clock = 500kHz with RT Resistor		50		ns
PLL Lock in Time		External Clock = 500kHz		100		μs
HIGH-SIDE MOSFET						
Minimum Controllable On Time	$T_{ON(MIN)}$	V_{IN} = 12V		200		ns

■ DETAILED DESCRIPTION

Overview

UTC **UD60501** is a 60V asynchronous buck converter with a maximum output current of 5A. The device achieves high efficiency operation through internally integrated low RDS(ON) NMOS. The fixed frequency peak current control mode is adopted to achieve fast response and simplify external compensation devices.

The device can set the frequency through the ground resistor of the RT/CLK pin, or inject an external clock signal into the RT/CLK pin and synchronize the SW rising edge with the clock falling edge through the internal PLL (phase-locked loop). The switching frequency can be set between 100KHz-2500KHz.

EN is enabled by an internal pull-up current source. The UVLO (input undervoltage lockout) threshold of the IC can be adjusted using the EN pin through external resistor. The default value is 4.3V.

Fixed-Frequency PWM Control

UTC **UD60501** adopts fixed frequency peak current control mode, and the switching frequency is adjustable. The voltage feedback loop adjusts the peak current through the reference voltage offset to obtain accurate DC voltage output. The output voltage is connected to the FB terminal through the sampling resistor and compared with the internal reference voltage. The switch current is controlled by the error amplifier inside the COMP terminal. The COMP voltage changes in a positive correlation with the switch current. The switch current is controlled by setting the clamp voltage for COMP.

Power Saving Mode

The UTC **UD60501** has a power-saving mode under light load conditions, which improves the overall efficiency of the device by reducing switching losses and drive losses.

The device enters the power-saving mode when the output voltage is within the specified range and the peak switch current at the end of each switching cycle is lower than the pulse skipping current threshold. In this mode, the COMP voltage is below the power-saving mode voltage threshold, the switch is inhibited, the output voltage decreases, and the voltage control loop responds to the drop in output voltage by increasing the COMP voltage. When the COMP voltage is above the pulse skipping threshold, the switch is enabled, the output voltage returns to the stable value, the COMP voltage returns below the power-saving mode voltage threshold, and the device enters the power-saving mode again.

It should be noted that the above peak current values are related to the power inductor value used. Therefore, the load current at which the device enters the power-saving mode depends on the inductance value.

The PLL module in the power-saving mode remains operational, and the switching transitions occur simultaneously with the external clock signal.

■ DETAILED DESCRIPTION(Cont.)

Adjusting Under voltage Lockout

The device is enabled when the V_{IN} port voltage is above 4.3V and the EN port voltage is above 1.2V (V_{ENTH}). The internal EN port has a current source of more than 1.2uA (I_P), which can enable the device when EN is suspended. If you want to adjust the higher UVLO threshold, you can do it by using two external resistors as shown in Figure 1. When the EN port voltage exceeds 1.2V, the port generates an additional 3.7μA (I_H) delay current. When the EN port voltage is lower than when it is below 1.2V, the delay current will be removed. According to the required starting voltage, the required resistance can be calculated by Equation 1, 2.

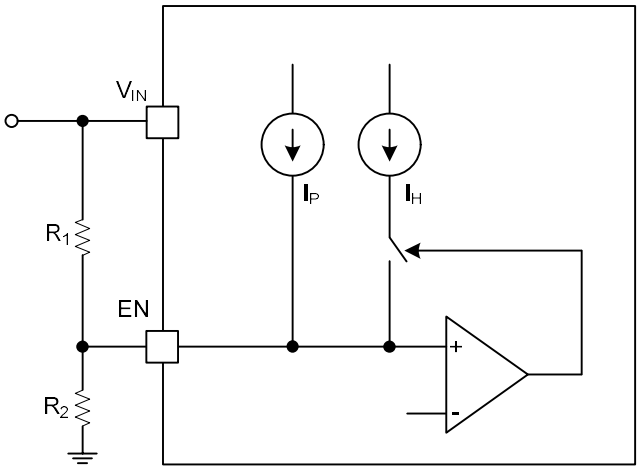


Figure 1. Adjustable V_{IN} Under-Voltage Lockout

$$R_1 = \frac{V_{START} - V_{STOP}}{I_H} \quad (1)$$

$$R_2 = \frac{V_{ENTH}}{\frac{V_{START} - V_{ENTH}}{R_1} + I_P} \quad (2)$$

Bootstrap Voltage and Low Dropout Operation

UTC **UD60501** reduces the number of external components by integrating a bootstrap charging diode. The capacitor between BOOT and SW provides the gate drive voltage for the high-side MOS. The voltage across the capacitor is monitored by a UVLO circuit. When the voltage difference between BOOT and SW is lower than the preset value (2.7V), the circuit turns off the high-side MOS, and the internally integrated low-side MOS pulls SW down to charge the BOOT capacitor. Since the gate drive current is small, the high-side MOS can keep switching for many cycles before each BOOT capacitor refresh. Therefore, the effective duty cycle of the device can be close to 100%.

Timing Resistor (RT/CLK) Terminal and Clock Synchronization

The switching frequency of UTC **UD60501** can be adjusted by setting a ground resistor on the RT/CLK pin or injecting the clock directly.

In the mode of setting the switching frequency by resistor, the switching frequency of the device can be adjusted between 100KHz-2500KHz. The relationship between the RT resistance value and the frequency can be calculated by equation 3.

$$f_{SW}(KHz) = \frac{100000}{R_T(K\Omega)^{0.991}} \quad (3)$$

■ DETAILED DESCRIPTION(Cont.)

In the mode of setting the switching frequency by external clock injection, the switching frequency of the device can be adjusted between 150KHz-2400KHz. There are two ways to inject the clock signal, as shown in Figure 2. The first method is suitable for low-impedance signal sources. The RT resistor is connected in parallel with the coupling capacitor (10pF ceramic capacitor is recommended) and grounded through the terminal resistor (for example, 50Ω). When the clock signal is turned off, the switching frequency is set by the series resistance of the two resistors. The second method is suitable for high-impedance signal sources. When the signal source is turned off, the switching frequency is set by the RT ground resistor.

For the clock square wave signal, its low level should be lower than 0.5V, the high level should be higher than 1.7V, and the pulse width should be greater than 30ns.

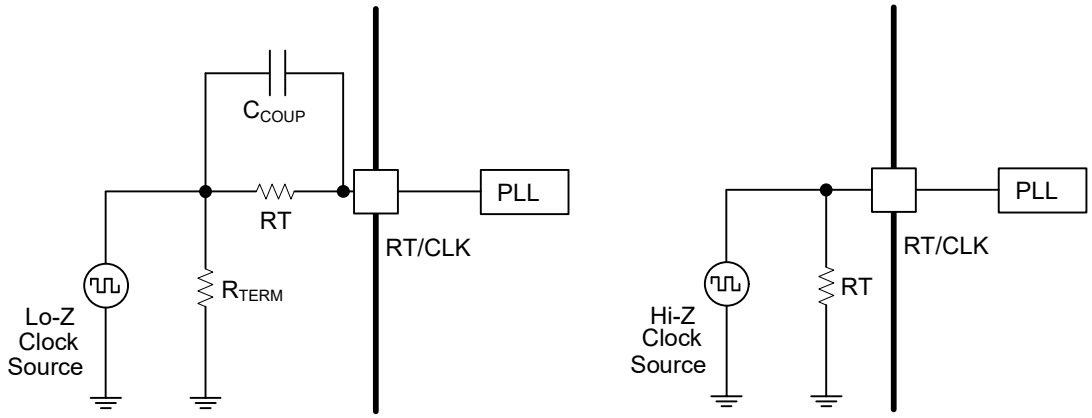


Figure 2. Setting Frequency and Clock Synchronization

When switching from RT resistor mode to clock injection mode, the PLL will lock the external clock signal within 100us, the internal 0.5V voltage will be removed, the RT/CLK pin will become high impedance, and the rising edge of SW will be synchronized with the falling edge of the clock signal. When switching from clock mode to RT resistor mode, a 0.5V bias voltage will be applied to the RT/CLK pin.

Soft-Start

UTC **UD60501** integrates digital soft-start circuit to reduce overshoot voltage and surge current that may occur during startup. The soft start will reset when EN is turned off and thermal shutdown occurs.

Over voltage Protection

In order to prevent the voltage overshoot that may occur during load transient or from output short circuit to no-load, UTC **UD60501** compares the FB pin voltage and OVP threshold through the overvoltage comparator in the internal OVP circuit. When the FB voltage is higher than the rising OVP threshold, the high-side MOS is immediately turned off to reduce the overshoot. When the FB voltage is lower than the falling OVP threshold, the high-side MOS can be turned on again.

Thermal Shutdown

In order to avoid equipment damage due to over-temperature, when the IC junction temperature exceeds the maximum threshold (typical 165°C), thermal shutdown will be triggered immediately and the device will stop working. Since the hysteresis value of temperature protection is approximately 10°C, that is, when the junction temperature is lower than 155°C, the device will automatically resume work through soft start.

■ APPLICATION INFORMATION

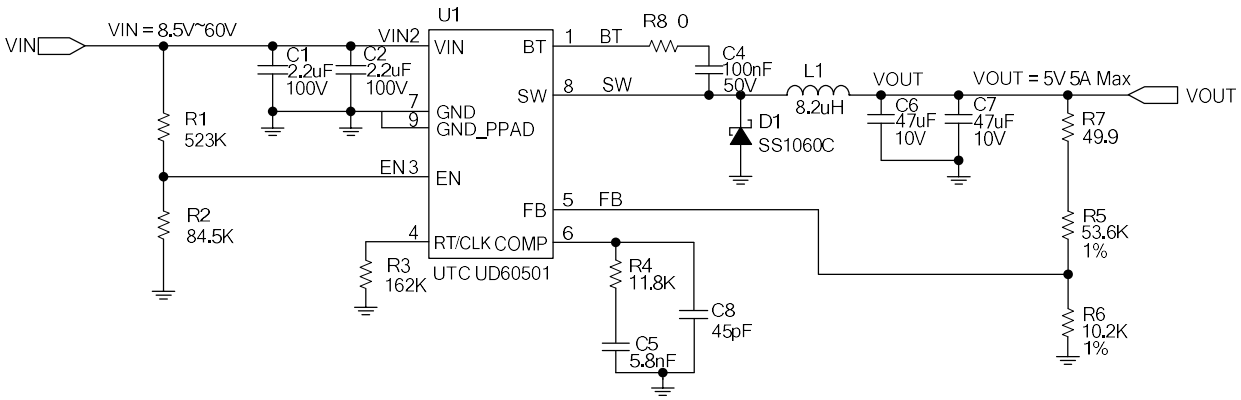


Figure 3. A Reference Design for 5V, 5A Application

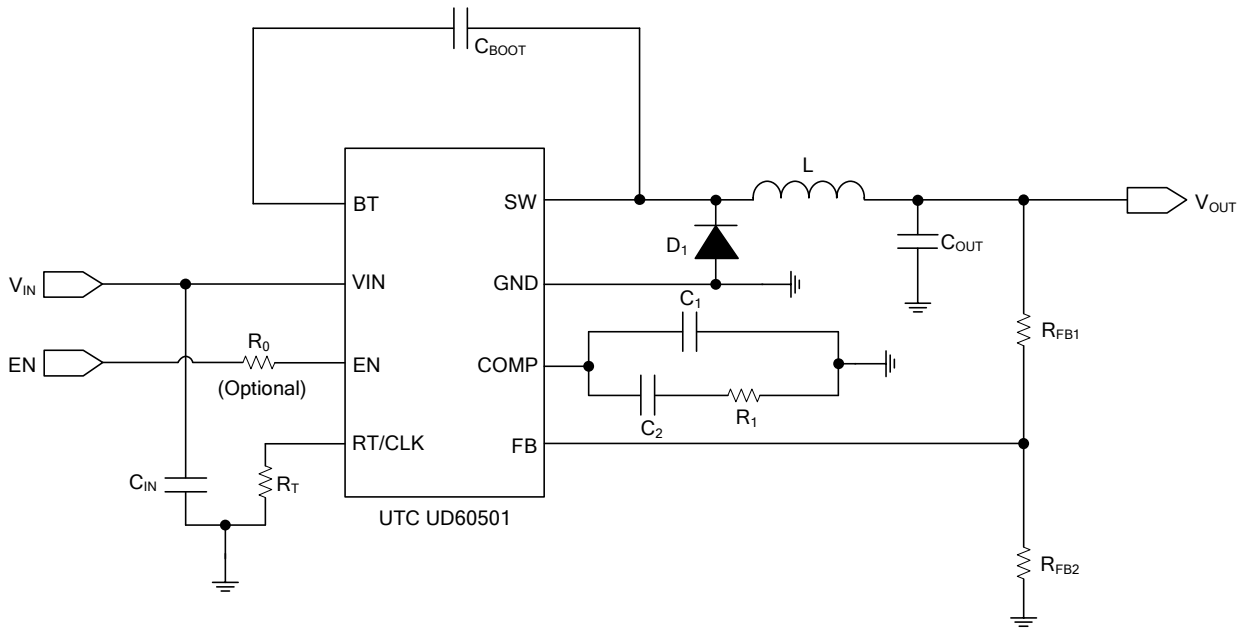
Design Requirements

- If needed, 1% resistors R5 and R6 can be selected to improve the accuracy of the output voltage.
- Increasing the resistance of R5 and R6 can improve the efficiency of the device under light load conditions. It should be noted that too high a resistance value will increase its sensitivity to noise.
- The maximum and minimum input voltages and operating frequencies supported under specific operating conditions are affected by the minimum on-time and minimum off-time of the switch.

Table 1. Recommended Component Values

VOUT(V)	F_{SW}(kHz)	R3(kΩ)	L1(μH)	COUT(μF)	CIN(μF)	R5(kΩ)	R6(kΩ)	R4(kΩ)	C5(nF)	C8(pF)
5	100	953	47	220	15*4	54.9	10.5	8.45	22	390
5	600	162	8.2	47*2	10*3	54.9	10.5	11.8	5.6	47
24			33	47*3	2.2*3	348	12	11.3	5.6	47
36			33	100+10	2.2*3	470	10.7	16.9	8.2	33
12	2500	39.2	3.3	47	4.7	147	10.5	15.8	1.8	8.2
24			5.6	47*3	2.2*3	348	12	34	3.9	3.9

■ TYPICAL APPLICATION CIRCUIT



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