



U74HCT2G08

CMOS IC

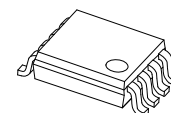
DUAL 2-INPUT AND GATE

■ DESCRIPTION

The **U74HCT2G08** is a 2-input AND gate which provides the Function $Y=A \times B$.

■ FEATURES

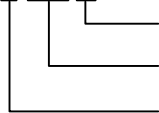
- * Operation Voltage Range: 4.0 ~ 5.5V
- * Overvoltage tolerant inputs to 6.0V
- * Symmetrical output impedance
- * Balanced propagation delays
- * CMOS low power dissipation
- * High noise immunity
- * Green & Pb Free



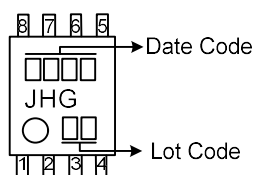
VSSOP-8

■ ORDERING INFORMATION

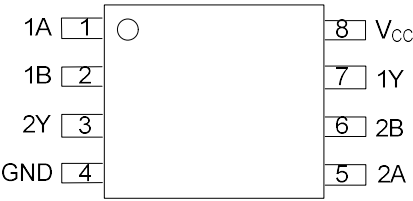
Ordering Number	Package	Packing
U74HCT2G08G-V08-R	VSSOP-8	Tape Reel

U74HCT2G08G-V08-R	
	(1) Packing Type (2) Package Type (3) Green Package
	(1) R: Tape Reel (2) V08: VSSOP-8 (3) G: Halogen Free and Lead Free

■ MARKING



PIN CONFIGURATION



PIN DESCRIPTION

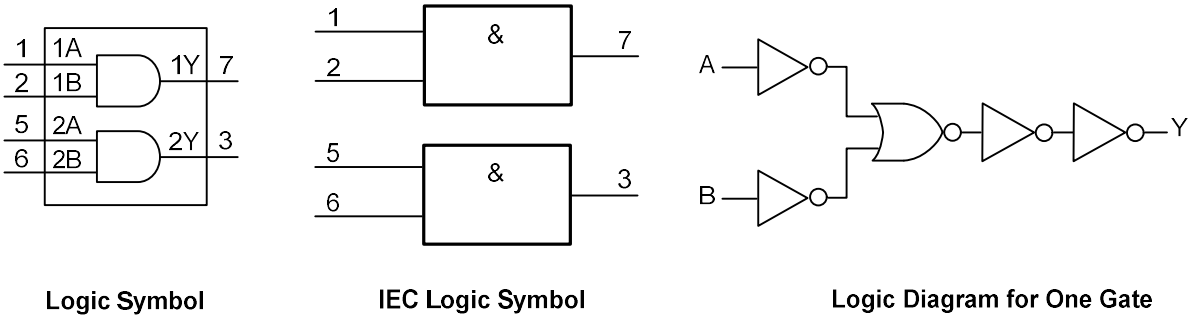
PIN NO.	PIN NAME	DESCRIPTION
1, 5	1A, 2A	Data input
2, 6	1B, 2B	Data input
4	GND	Ground (0V)
3, 7	2Y, 1Y	Data output
8	V _{CC}	Supply voltage

FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level, L = LOW voltage level.

LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified) (Note 1, 2)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ +7.0	V
Input Voltage	V _{IN}		-0.5 ~ +7.0	V
V _{CC} or GND Current	I _{CC}		±50	mA
Continuous Output Current	I _{OUT}	-0.5V < V _{CC} +0.5V	±25	mA
Input Clamp Current	I _{IK}	V _{IN} < -0.5V or V _{OUT} > +0.5V	-20	mA
Output Clamp Current	I _{OK}	V _{OUT} < -0.5V or V _{OUT} > +0.5V	±20	mA
Ground Current	I _{GND}		-50	mA
Power Dissipation	P _D		250	mW
Storage Temperature	T _{STG}		-65 ~ + 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. It's guarantee by design, this parameter is not production tested.

■ RECOMMENDED OPERATING CONDITIONS (NOTE)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		4.0		5.5	V
Input Voltage	V _{IN}		0		V _{CC}	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Input Transition Rise or Fall Rate	Δt/ΔV	V _{CC} =4.5V		1.67	139	ns/V
Operating Temperature	T _A		-40		+125	°C

Note: It's guarantee by design, this parameter is not production tested.

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V _{IH}	V _{CC} =4.5V ~ 5.5V	2.0			2.0			V
Low-Level Input Voltage	V _{IL}	V _{CC} =2V			0.8			0.8	V
High-Level Output Voltage	V _{OH}	V _{CC} =4.5V, I _{OH} =-20μA	4.4			4.4			V
		V _{CC} =4.5V, I _{OH} =-4mA	4.13			3.7			V
Low-Level Output Voltage	V _{OL}	V _{CC} =4.5V, I _{OH} =-20μA			0.1			0.1	V
		V _{CC} =4.5V, I _{OH} =-4mA			0.33			0.4	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =5.5V V _{IN} =V _{CC} or GND			±1			±1	μA
Supply Current	I _{CC}	V _{CC} =6.0V V _{IN} =V _{CC} or GND, I _{OUT} =0A			1			40	μA
Additional Supply Current	ΔI _{CC}	V _{CC} =4.5V ~ 5.5V V _{IN} = V _{CC} -2.1V, I _o =0A			375			410	μA
Input Capacitance	C _{IN}			1.5					pF

Note: It's guarantee by design, this parameter is not production tested.

■ DYNAMIC CHARACTERISTICS (Input: t_R , $t_F=6\text{ns}$, unless otherwise specified)

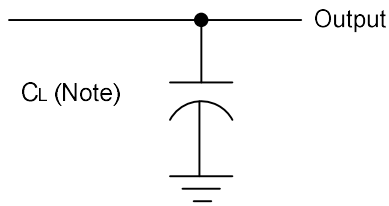
PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ\text{C}$			$T_A=-40\sim+125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (A and B) to Output (Y)	t_{PHL}/t_{PLH}	$V_{CC}=4.5\text{V}$, $C_L=50\text{pF}$			30			36	ns
		$V_{CC}=5.5\text{V}$, $C_L=50\text{pF}$			27			33	ns
Output Transition Time	t_{THL}/t_{TLH}	$V_{CC}=4.5\text{V}$, $C_L=50\text{pF}$			19			22	ns
		$V_{CC}=5.5\text{V}$, $C_L=50\text{pF}$			16			19	ns

Note: It's guarantee by design, this parameter is not production tested.

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No Load		10		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.

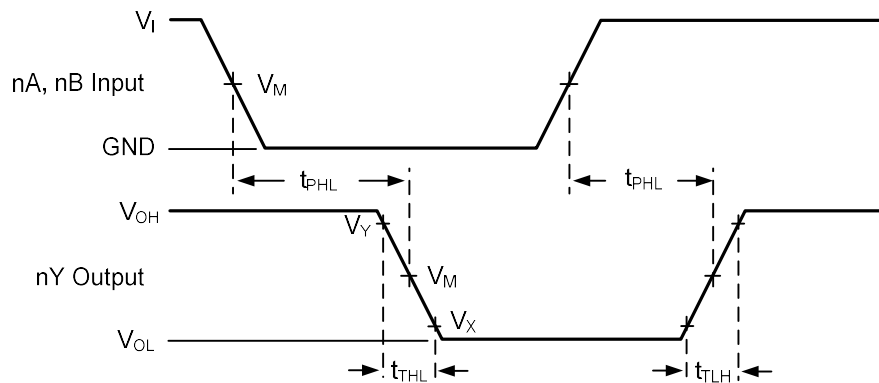
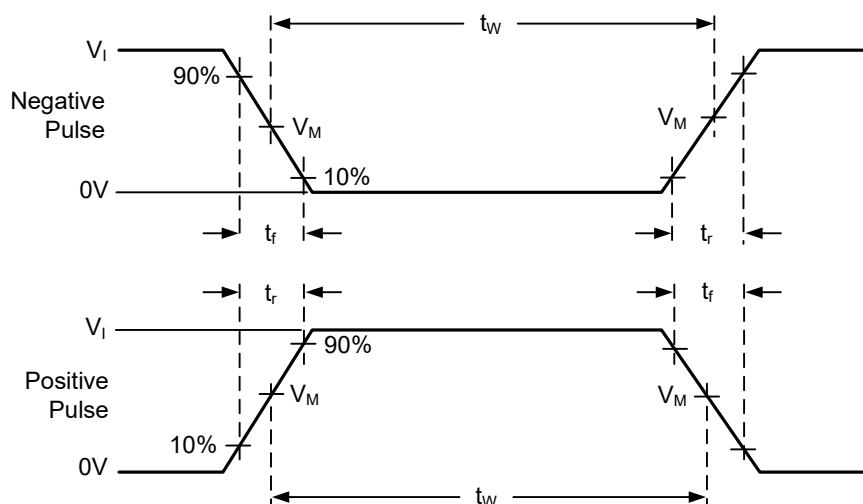


Figure 1. The input (nA and nB) to output (nY) propagation delays

INPUT	OUTPUT		
V_M	V_M	V_X	V_Y
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



■ TEST CIRCUIT AND WAVEFORMS (Cont.)

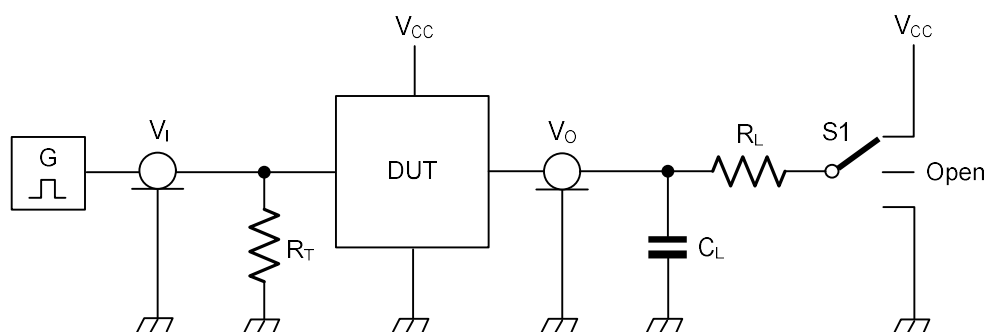


Figure 2. Test circuit for measuring switching times

INPUT		LOAD		S1 POSITION
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
GND to 3V	$\leq 6 \text{ ns}$	15pF, 50pF	1k Ω	Open

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