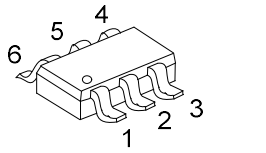
4.5V TO 48V, 1A, 650KHz SYNCHRONOUS STEP-DOWN CONVERTER



SOT-26

■ DESCRIPTION

The UTC **UD48101A** is an easy to use synchronous stepdown Buck, which integrated with highside and low-side power MOSFETs. The UTC **UD48101A** can provide up to 1A of output current efficiently with current-mode control for fast loop response.

Wide 4.5V to 48V input range accommodates a variety of power meter step-down applications. UTC **UD48101A** uses high duty cycle and low dropout mode for low power meter input voltage conditions.

The UTC **UD48101A** achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

The UTC **UD48101A** has built-in full protection features, cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation.

■ FEATURES

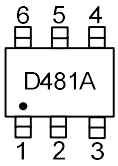
* 4.5V to 48V Input Voltage Range
* 50V Absolute Maximum Rating
* 1A Continuous Output Current
* 100ns Minimum Switching-On Time
* 2%~98% Large Range Duty Cycle
* Stable with Ceramic/Electrolytic Output Capacitors
* 650KHz Switching Frequency
* Light Load Pulse Frequency Modulation
* 420mΩ/220mΩ Internal Power MOSFETs
* Support Startup with Pre-Biased Output
* Short Circuit Protection with Hiccup Mode
* ±1.5% Tolerance Voltage Reference at 25°C
* Output Voltage Adjustable from 0.8V
* Precision Enable
* Over Temperature Protection
* Green & Pb Free

■ ORDERING INFORMATION

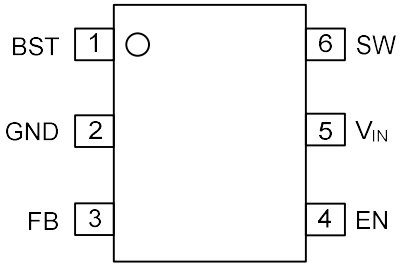
Ordering Number	Package	Packing
UD48101AG-AG6-R	SOT-26	Tape Reel

UD48101AG-AG6-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G : Halogen Free and Lead Free

■ MARKING



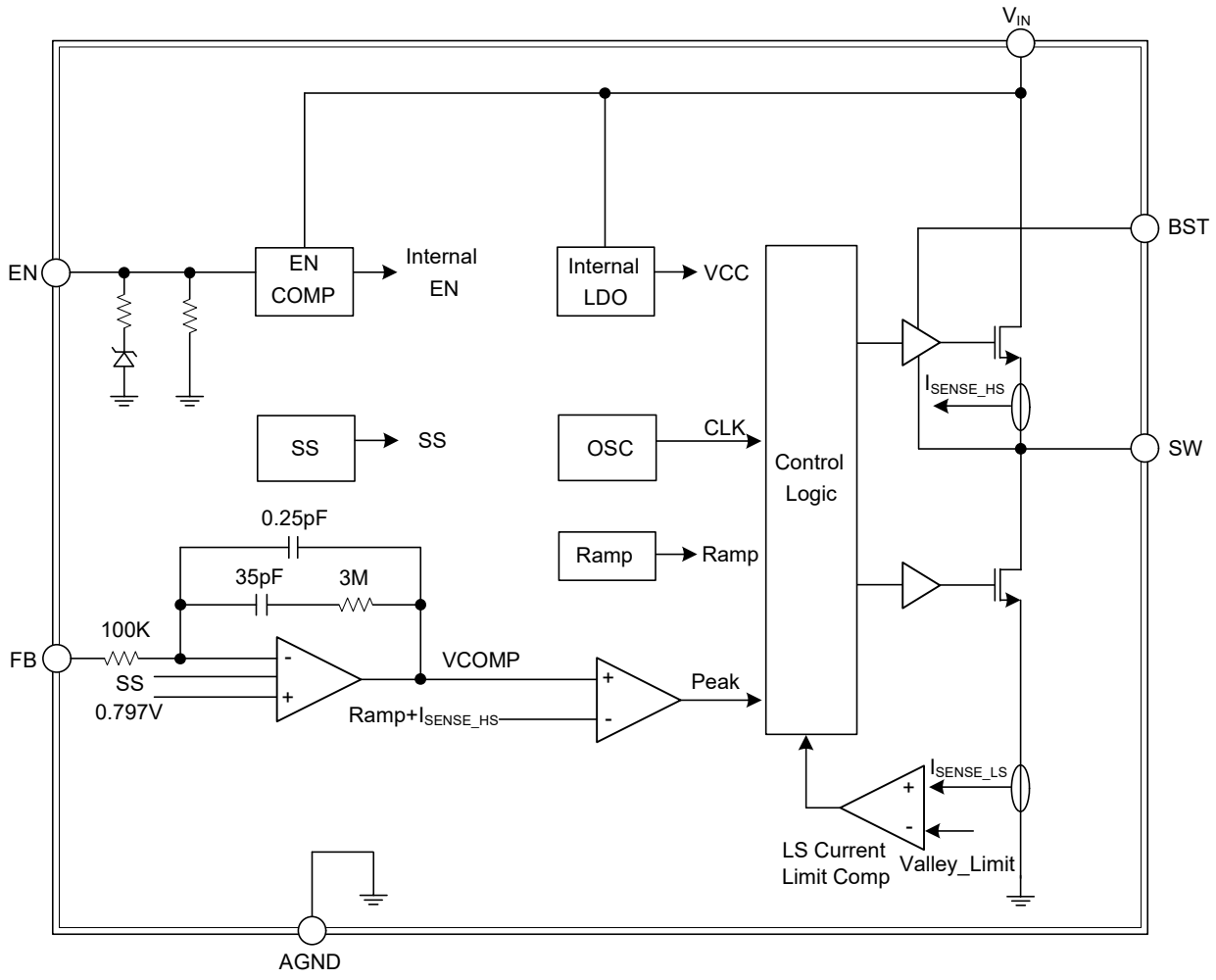
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	BST	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	GND	Power Ground terminal.
3	FB	Feedback input to the convertor. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
4	EN	Precision enable input to the convertor. High = on, Low or float = off. Can be tied to V_{IN} by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
5	V_{IN}	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
6	SW	Switching output of the converter. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	-0.3 ~ 50	V
SW to GND	SW	-0.7 (-5V in 10ns) ~ V_{IN} + 0.7	V
EN to GND	EN	50	V
BST to SW	BST	-0.3 ~ 6	V
All Other Pins		-0.3 ~ 6	V
Junction Temperature	T_J	-40 ~ +150	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
BST to SW	BST	4 ~ 5	V
FB to GND	FB	0 ~ 1	V
V_{IN} to GND	V_{IN}	4.5 ~ 48	V
V_{OUT} to GND	V_{OUT}	0.8 ~ 0.98 × V_{IN}	V
Max Continuous Output Current	I_{OUT}	1	A

■ THERMAL RESISTANCE (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient Thermal Resistance	θ_{JA}	100	°C/W
Junction to Case Thermal Resistance	θ_{JC}	55	°C/W

Note: Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{FB}	T_J = -40°C ~ +125°C	781	797	813	mV
		T_J = +25°C	785	797	809	mV
Feedback Leakage	I_{LK_FB}	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
High-Side Switch on Resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		420	840	mΩ
Low-Side Switch on Resistance	R_{ON_LS}	V_{IN} = 15V		220	440	mΩ
High-Side Switch Leakage	LKG_{HS}	V_{EN} = 0V, V_{SW} = 0V			1	μA
Low-Side Switch Leakage	LKG_{LS}	V_{EN} = 0V, V_{SW} = 45V			1	μA
High-Side Current Limit	I_{LIM_HS}			2		A
Low-Side Current Limit	I_{LIM_LS}		0.9	1.1	1.3	A
V_{IN} UVLO Rising Threshold	V_{IN_UVR}		4.15	4.3	4.45	V
V_{IN} UVLO Falling Threshold	V_{IN_UVF}		3.85	4.05	4.25	V
V_{IN} UVLO Hysteresis	$V_{IN\_UV\_hys}$			0.3		V
Soft-Start Time	T_{SS}	V_{FB} from 10% to 90%	0.35	0.6	0.85	ms
Oscillator Frequency	f_{SW}			650		KHz
Minimum Switch On Time (Note 1)	t_{ON_MIN}			100		ns
Maximum Switch On Time (Note 1)	t_{ON_MAX}			5.2		μs
Minimum Switch Off Time (Note 1)	t_{OFF_MIN}			92		ns
Shutdown Supply Current	I_{QS}	V_{EN} < 0.3V, V_{IN}=15V		1	2	μA
Quiescent Supply Current	I_Q	No Load, V_{FB} = 0.83V, No Switching		150	220	μA
Enable Rising Threshold	V_{EN_R}	Low to high	1.5	1.55	1.6	V
Enable Falling Threshold	V_{EN_F}	High to low	1.1	1.22	1.3	V
Enable Threshold Hysteresis	V_{EN_Hys}			0.3		V
Thermal Shutdown (Note 1)	T_{OTP_R}			151		°C
Thermal Shutdown Hysteresis (Note 1)	T_{OTP_Hys}			21		°C

Note: 1. Not tested in production and derived from bench characterization.

■ FUNCTION DESCRIPTIONS

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, UTC **UD48101A** operates in a fixed-frequency, peak current control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle initiated by the internal clock turns on the power high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). After the HS- FET is off, the low-side MOSFET (LS-FET) turns on, and the inductor current flows through the LS-FET. To avoid a shoot-though, a dead time is inserted to prevent the HS-FET and LS- FET from turning on at the same time. For each turn-on and turn-off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

To prevent inductor current and output voltage runaway, the switching frequency folds back when the HS-FET minimum turn-on is detected internally. When the PWM signal goes low, the HS-FET turns off and remains off for at least 110ns before the next cycle begins. If the current in the HSFET does not reach the COMP-set current value within one PWM cycle, the HS- FET remains on a max on time to avoid a turn-off operation.

If the input voltage is too high, the on time will be short, getting close to the min on time. When the duty needs to be smaller than 2%, the UTC **UD48101A** will keep the on time as min on time and extend the off time to regulate the output voltage, and keep stable and nice output ripple.

When the UTC **UD48101A** works in pulse-frequency modulation (PFM) mode during light-load operation, the UTC **UD48101A** reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver enters tri-state (high-Z). The output capacitors discharge slowly to GND through R1 and R2. When VFB drops below the reference voltage, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.7MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN can connected to V_{IN} directly.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UTC **UD48101A** UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.3V, while its falling threshold is about 4V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 0.6ms internally.

When UTC **UD48101A** startup with large output capacitor, IC current limit will be triggered which will limit the output rising slew rate. To avoid false trigger the hiccup protection with large output capacitor during startup period. UTC **UD48101A** internal soft star time will be automatically extended in this condition.

Large Duty Cycle Operation

When UTC **UD48101A** will automatically extend the frequency to support the application when V_{IN} is close to V_{OUT}. The frequency extend circuit will be triggered when Toff min time is reached. The UTC **UD48101A** can support up to 98% maximum duty cycle.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The UTC **UD48101A** has both valley current-limit control and peak current limit control. During LS-FET on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS-FET limit comparator. The device enters overcurrent protection (OCP) mode, and the HS-FET waits until the valley current limit disappears before turning on again. During the HS-FET on period, the inductor current is sensed and compare with the peak current-limit. If the peak current limit is triggered, the ON pulse will be terminated immediately. The output voltage drops until V_{FB} is below the under voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the UTC **UD48101A** enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

■ FUNCTION DESCRIPTIONS (Cont.)

Pre-Bias Start-Up

The UTC **UD48101A** is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature falls below its lower threshold, the chip is enabled again.

■ APPLICATION INFORMATION

Setting the Output Voltage

The UTC **UD48101A** output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.797V. The feedback network is shown below Figure 1.

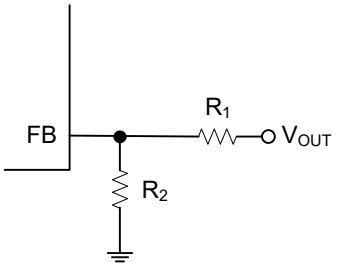


Figure 1. Feedback Network

Choose R1 and R2 using Equation (1):

$$V_{OUT}=V_{FB}\ (R1+R2)\ /\ R2 \quad (1)$$

Selecting the Inductor

For most applications, use a 1μH to 47μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance.

For most designs, the inductance value can be derived from Equation (2):

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times F_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)}=I_{LOAD}+\frac{\Delta I_L}{2} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1. Resistor Selection for Common Output Voltages (7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)
5	604	115	20	22
3.3	604	191	20	22

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (4):

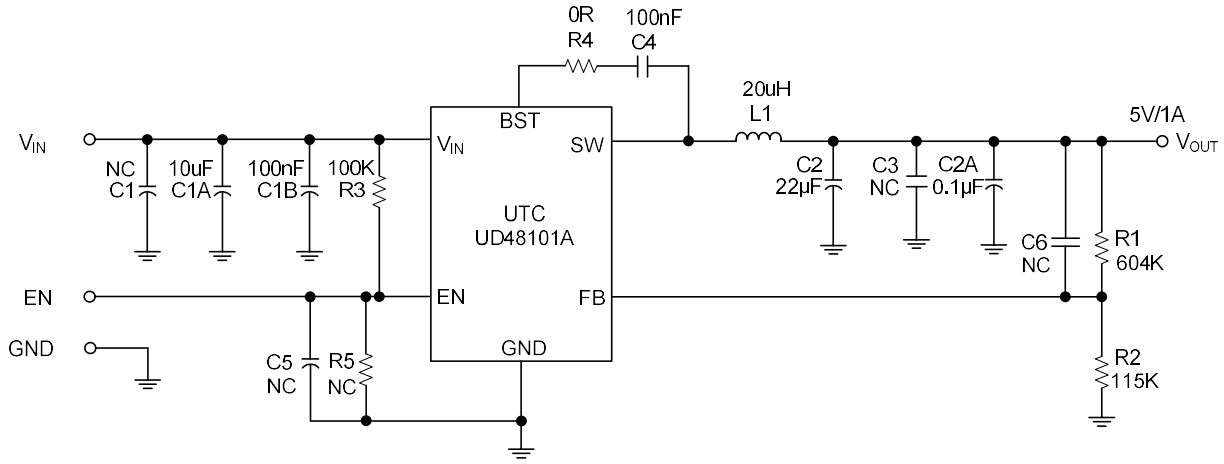
$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times F_{OSC}\times C_{OUT}}\right) \quad (4)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

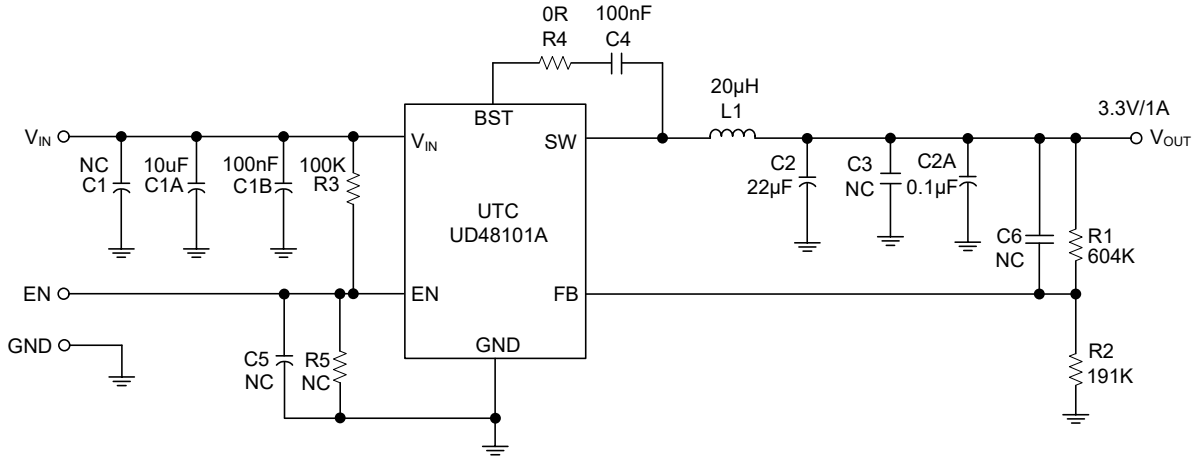
The characteristics of the output capacitor also affect the stability of the regulation system. The UTC **UD48101A** can be optimized for a wide range of capacitance and ESR values.

■ TYPICAL APPLICATION CIRCUITS

V_{IN}=12V, V_{OUT}=5V/1A



V_{IN}=12V, V_{OUT}=3.3V/1A



■ TYPICAL APPLICATION