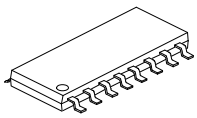
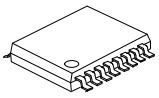
U74HC595D

CMOS IC

8-BIT SERIAL-IN SHIFT REGISTER WITH LATCHED 3-STATE PARALLEL OUTPUTS, PROVIDING SERIAL OUTPUT



SOP-16



TSSOP-16

■ DESCRIPTION

The UTC **U74HC595D** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output. The Serial Data Input (SER) will shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

■ FEATURES

* Operation Voltage Range: 2V ~ 6V
* High Noise Immunity
* Output Compatibility with CMOS and TTL
* Specified from -40°C ~ +125°C
* Green & Pb Free
* The output state will depend on the clock state immediately after power-up

■ ORDERING INFORMATION

Ordering Number	Package	Packing
U74HC595DG-S16-R	SOP-16	Tape Reel
U74HC595DG-P16-R	TSSOP-16	Tape Reel

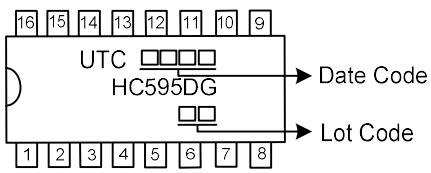
U74HC595DG-S16-R

(1)Packing Type — (1) R: Tape Reel

(2)Package Type — (2) S16: SOP-16, P16: TSSOP-16

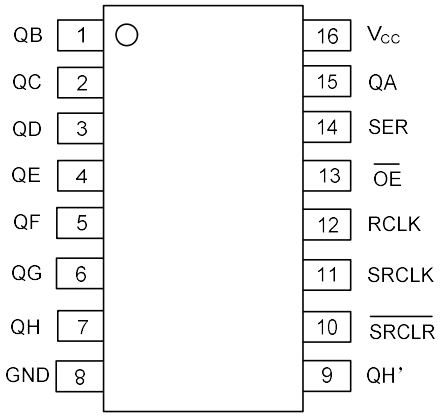
(3)Green Package — (3) G: Halogen Free and Lead Free

■ MARKING



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■ PIN CONFIGURATION



■ PIN DESCRIPTION

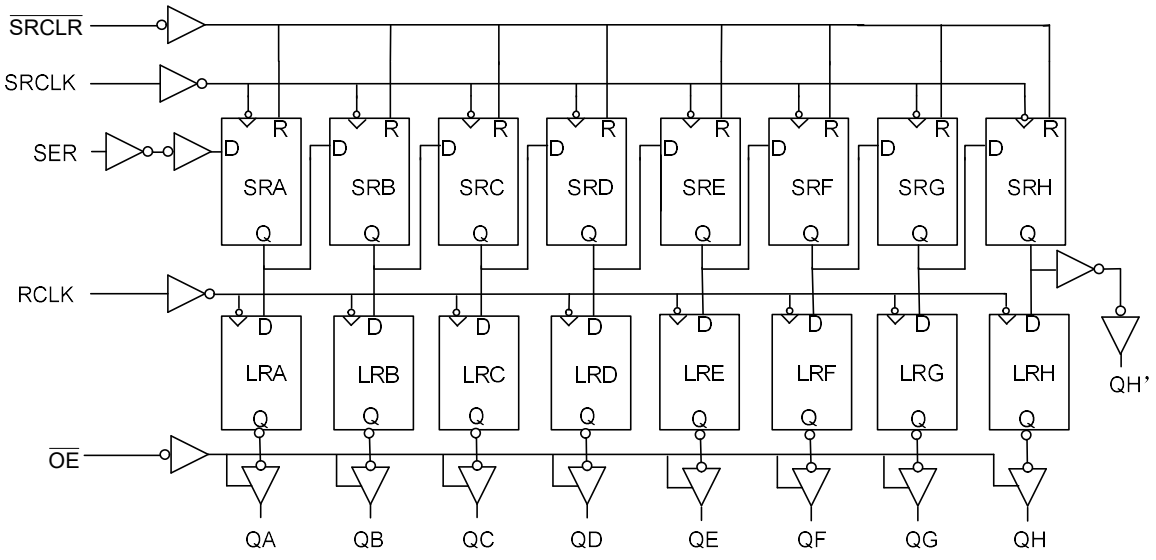
PIN NO.	PIN NAME	DESCRIPTION
1 ~ 7,15	QA~QH	Parallel data output
8	GND	Ground
9	QH'	Serial data output
10	$\overline{\text{SRCLR}}$	Shift register clear, active low
11	SRCLK	Shift register clock, rising edge triggered
12	RCLK	Storage register clock, rising edge triggered
13	$\overline{\text{OE}}$	Output enable, active low
14	SER	Serial data input
16	V_{CC}	Supply voltage

■ FUNCTION TABLE

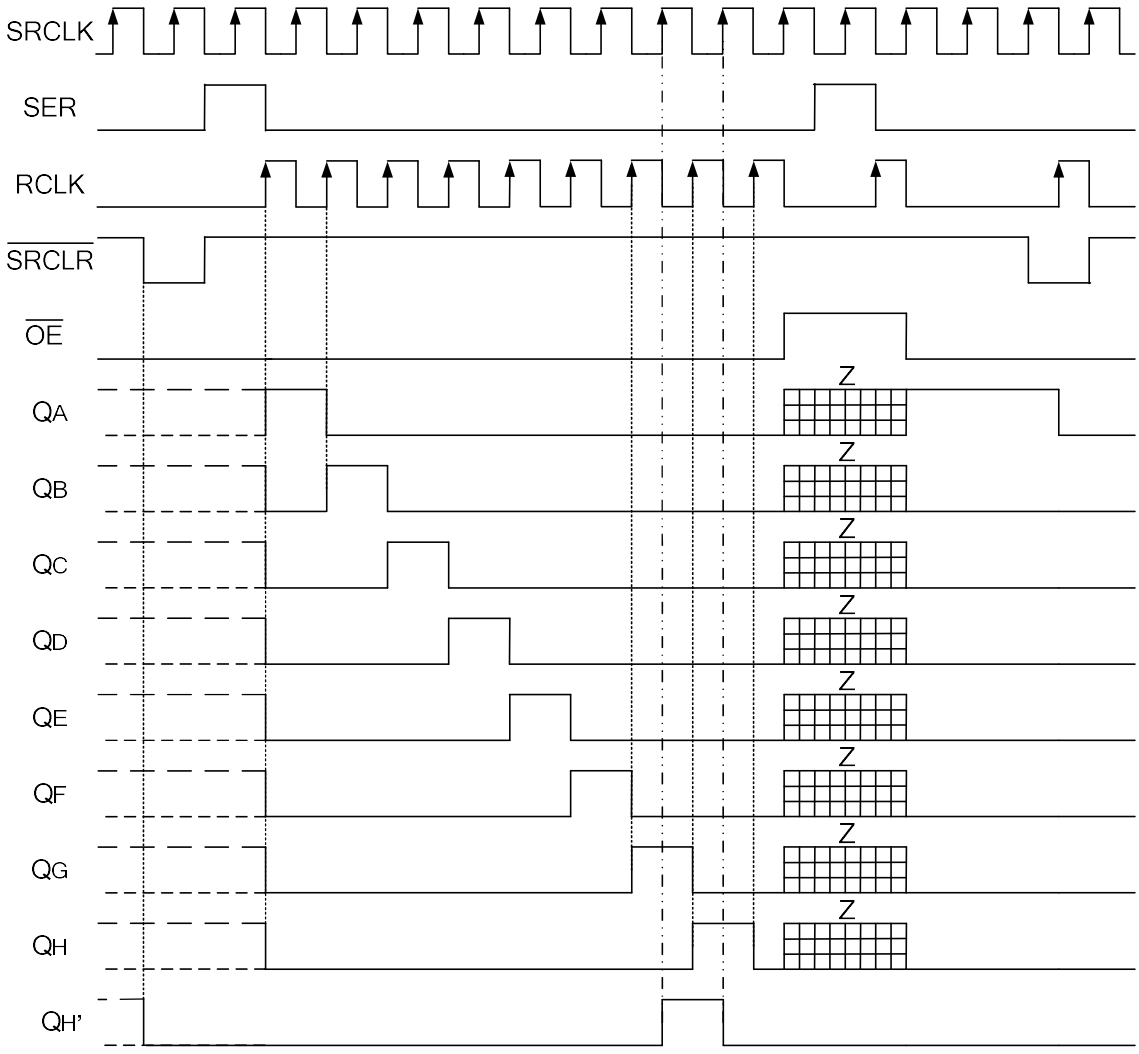
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note: H : HIGH voltage level.
L : LOW voltage level.
X : Don't care.
Z : High impedance OFF-state.
NC: No change.
↑ : Low-to-High transition.
↓ : High-to-Low transition.

■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified) (Note1,3)

PARAMETER		SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage		V_{CC}		-0.5 ~ 7.0	V
Input Clamp Current (Note 2)		I_{IK}	V_{IN} < 0 or V_{IN} > V_{CC}	±20	mA
Output Clamp Current (Note 2)		I_{OK}	V_{OUT} < 0 or V_{OUT} > V_{CC}	±20	mA
Output Current		I_{OUT}	V_{OUT} = 0 to V_{CC}	±35	mA
V_{CC} or GND Current		I_{CC}		±75	mA
Power Dissipation	DIP-16	P_D		500	mW
	TSSOP-16			450	mW
Electrostatic Discharge		$V_{(ESD)}$	Human-Body Model (HBM) Per JESD22-A114/115	2000	V
Storage Temperature		T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. It's guarantee by design, this parameter is not production tested.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2		6	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+125	°C
Input Transition Rise or Fall Time	t_R / t_F	V_{CC}=2V			200	ns
		V_{CC}=4.5V			100	ns
		V_{CC}=6V			100	ns

Note: It's guarantee by design, this parameter is not production tested.

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V_{IH}	V_{CC}=2V	1.5			1.5			V
		V_{CC}=3V	2.1			2.1			V
		V_{CC}=4.5V	3.15			3.15			V
		V_{CC}=6V	4.2			4.2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=2V			0.5			0.5	V
		V_{CC}=3V			0.9			0.9	V
		V_{CC}=4.5V			1.35			1.35	V
		V_{CC}=6V			1.8			1.8	V
High-Level Output Voltage, Q_A-Q_H	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	2.0		1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9	6.0		5.9			V
		V_{CC}=3V, I_{OH}=-2.4mA	2.48			2.3			V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98			3.7			V
		V_{CC}=6V, I_{OH}=-7.8mA	5.48			5.2			V
Low-Level Output Voltage, Q_A-Q_H	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=3V, I_{OL}=2.4mA			0.26			0.4	V
		V_{CC}=4.5V, I_{OL}=6mA			0.26			0.4	V
		V_{CC}=6V, I_{OL}=7.8mA			0.26			0.4	V
High-Level Output Voltage, Q_H'	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	2.0		1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9	6.0		5.9			V
		V_{CC}=3V, I_{OH}=-2.4mA	2.48			2.3			V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98			3.7			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48			5.2			V
Low-Level Output Voltage, Q_H'	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=3V, I_{OL}=2.4mA			0.26			0.4	V
		V_{CC}=4.5V, I_{OL}=4mA			0.26			0.4	V
		V_{CC}=6V, I_{OL}=5.2mA			0.26			0.4	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}=V_{CC} or GND			±0.1			±1	μA
Output Off-State Current	I_{OZ}	V_{CC}=6V, V_{OUT}=V_{CC} or GND			±0.5			±10	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8			160	μA

Note: It's guarantee by design, this parameter is not production tested.

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Pulse Frequency	f_{max}	V_{CC}=2V	C_L=50pF	5	10		3			MHz
		V_{CC}=4.5V		15	30		9			MHz
		V_{CC}=6V		18	35		12			MHz
Propagation Delay From Input (SRCLK) to Output ($Q_{H'}$)	t_{PD}	V_{CC}=2V	C_L=50pF		95	160			285	ns
		V_{CC}=4.5V			30	60			100	ns
		V_{CC}=6V			25	50			80	ns
Propagation Delay From Input (RCLK) to Output (Q_A-Q_H)		V_{CC}=2V	C_L=50pF		50	140			265	ns
		V_{CC}=4.5V			18	28			53	ns
		V_{CC}=6V			10	24			45	ns
		V_{CC}=2V	C_L=150pF		70	200			250	ns
		V_{CC}=4.5V			26	40			50	ns
		V_{CC}=6V			13	34			43	ns
Propagation Delay From Input ($\overline{SRCLR}$) to Output ($Q_{H'}$)	t_{PHL}	V_{CC}=2V	C_L=50pF		80	145			265	ns
		V_{CC}=4.5V			20	50			90	ns
		V_{CC}=6V			15	45			80	ns
Propagation Delay From Input ($\overline{OE}$) to Output (Q_A-Q_H)	t_{en}	V_{CC}=2V	C_L=50pF		37	135			225	ns
		V_{CC}=4.5V			17	27			45	ns
		V_{CC}=6V			9	23			38	ns
		V_{CC}=2V	C_L=150pF		55	200			250	ns
		V_{CC}=4.5V			22	40			50	ns
		V_{CC}=6V			15	34			43	ns
Propagation Delay From Input ($\overline{OE}$) to Output (Q_A-Q_H)	t_{dis}	V_{CC}=2V	C_L=50pF		30	150			250	ns
		V_{CC}=4.5V			13	30			50	ns
		V_{CC}=6V			8	26			43	ns
Output Transition Time (Q_A-Q_H)	t_t	V_{CC}=2V	C_L=50pF		30	60			75	ns
		V_{CC}=4.5V			9	12			15	ns
		V_{CC}=6V			6	10			13	ns
		V_{CC}=2V	C_L=150pF		72	210			265	ns
		V_{CC}=4.5V			25	42			53	ns
		V_{CC}=6V			15	36			45	ns
Output Transition Time ($Q_{H'}$)		V_{CC}=2V	C_L=50pF		28	75			95	ns
		V_{CC}=4.5V			12	15			19	ns
		V_{CC}=6V			6	13			16	ns

Note: It's guarantee by design, this parameter is not production tested.

■ TIMING REQUIREMENTS

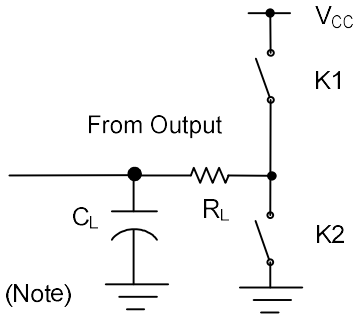
PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse Duration, SRCLK or RCLK High or Low	t_W	V_{CC}=2V	80			110			ns
		V_{CC}=4.5V	16			22			ns
		V_{CC}=6V	14			19			ns
Pulse Duration, $\overline{\text{SRCLR}}$ Low		V_{CC}=2V	80			110			ns
		V_{CC}=4.5V	16			22			ns
		V_{CC}=6V	14			19			ns
Setup Time, SER Before SRCLK↑	t_{SU}	V_{CC}=2V	100			125			ns
		V_{CC}=4.5V	20			25			ns
		V_{CC}=6V	17			21			ns
Setup Time, SRCLK↑ Before RCLK↑		V_{CC}=2V	75			94			ns
		V_{CC}=4.5V	15			19			ns
		V_{CC}=6V	13			16			ns
Setup Time, $\overline{\text{SRCLR}}$ Low Before RCLK↑		V_{CC}=2V	50			65			ns
		V_{CC}=4.5V	10			13			ns
		V_{CC}=6V	9			11			ns
Setup Time, $\overline{\text{SRCLR}}$ High (Inactive) Before SRCLK↑		V_{CC}=2V	50			60			ns
		V_{CC}=4.5V	10			12			ns
		V_{CC}=6V	9			11			ns
Hold Time, SER After SRCLK↑	t_H	V_{CC}=2V	3			3			ns
		V_{CC}=4.5V	3			3			ns
		V_{CC}=6V	3			3			ns

Note: It's guarantee by design, this parameter is not production tested.

■ OPERATING CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=6V, V_{IN}=V_{CC} or GND			10	pF
Power Dissipation Capacitance	C_{PD}	No load		400		pF

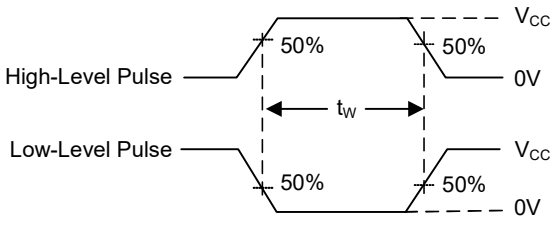
■ TEST CIRCUIT AND WAVEFORMS



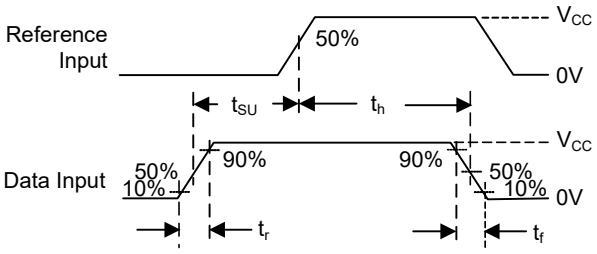
TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

t_{PD} is the same as t_{PHL} and t_{PLH}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

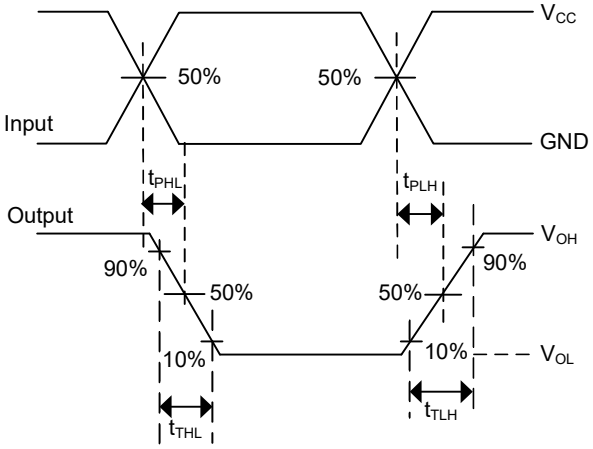
Note: C_L includes probe and jig capacitance. C_L=50pF or 150pF, R_L=1KΩ



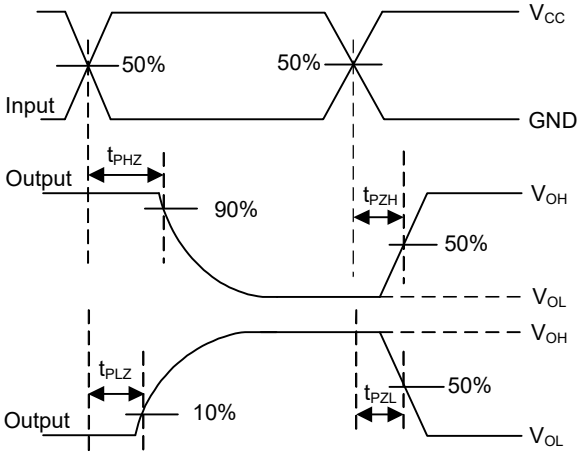
Voltage Waveforms, Pulse Duration



Voltage Waveforms



Voltage Waveforms Propagation Delays



Voltage Waveforms Propagation Delays

Note: All input pulses are supplied by generators having the following characteristics:
P_{RR} ≤ 1MHZ, Z_O = 50Ω, t_r ≤ 3ns, t_f ≤ 3ns.

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